User's Manual

EMMA Mobile Family
SEMC-EM1

EMMA Mobile^{TM}1 Development Kit Board

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[MEMO]

These commodities, technology or software, must be exported in accordance with the export administration regulations of the exporting country. Diversion contrary to the low of that country is prohibited.

NOTES FOR CMOS DEVICES

1. Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

2.HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3.PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4.STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5.POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device. INPUT OF SIGNAL DURING POWER OFF STATE Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be

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PREFACE

(1) Readers
This manual is intended for hardware/software application system designers who wish to understand and use board functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

(2) Purpose
This manual is intended to explain to users the hardware and software functions of the board of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

(3) Organization
This manual consists of the following chapters.

- Chapter 1 Introduction
- Chapter 2 Functions
- Chapter 3 System Control
- Chapter 4 Connecters
- Chapter 5 Others

(4) How to read this manual
It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.
To understand the functions of the board of EM1 in detail, read this manual according to the CONTENTS.
To understand the LSI functions of EM1, refer to the user's manual of the respective module.
To understand the electrical specifications of EM1, refer to the Data Sheet.

(5) Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with Note in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB Decimal ... xxxx Hexadecimal ... xxxxH
Data type:	Word … 32 bits Half word … 16 bits Byte … 8 bits

(6) Major revised point
The revised points can be easily searched by using an "<R>" in the PDF file and specifying it in the "Find what:" field.

DISCLAIMER

This user's manual and development kit board is intended for the evaluation of the Emma mobile 1 and is not intended to be included as part of any final product. The designs contained in this document are for reference and example purposes only.
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Related Documents

Document Name		Document No.
Data sheet		S19269E
User's Manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	Power Supply Chip	S19360E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip	S19268E

Caution: The related documents listed above are subject to change without notice. The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Be sure to use the latest version of each document when designing.

CONTENTS

LIST OF FIGURES

LIST OF TABLE

To use this Product safety

In this paragraph, it explains notes to use this product safety. Please read before using the product.
・Please defend the content of the description of this document and use the product.
・Please keep this document near the main body of the product to refer at once when it is necessary.
・The content that has been described is the one in this document at the time of making. The inquired window, address, telephone number, and the content and the address, etc. on the homepage might have been changed. Please acknowledge it beforehand.

To mean mark

In this document, the item to use the product safety has been described as follows.

■When you cannot defend the content of the description. You damage to personal to harm and the property.

 **DANGER**	It is assumed that the user owes the death or the serious illness (note 1) and shows the content with high risk.
 **WARNING**	The content that the user owes the death or the serious illness is shown.
 **CAUTION**	The people receive injury (note 2), Receive the property damage (note 3).

（note１） Definition of serious illness. Losing sight, injury, Burn (high temperature and low temperature), Electric shock, Fracture, The one that squealed remains because of poisoning etc and the one to require going to hospital regularly that hospitalizes and is long-term to treat.

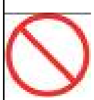
（note 2 ）Definition of injury. The one to require hospitalization and a long-term going to hospital regularly to treat is said.

（note ３）Definition of property damage. It is damage to the building and equipment.

Alarm display in board products use

■The demand in the handling of the product is classified as follows.

・It is a mark that prohibits the act.

	General prohibition The described act is prohibited.		Example: Contact prohibition The possibility of owing injury by touching the specific location is shown.

・It is a mark of attention.

	General attention The general attention not specified is shown.		Example: High temperature attention. The possibility of injury by the high temperature is shown.

・It is a mark that compels the act based on the instruction.

	General instruction It is the one to compel the act based on the instruction.		The example: Pull out the power plug. It is the one directed to pull out the plug of the AC adapter.

DANGER

DANGER	
	There is no danger marking in this product.

Warning

Warning	
	The hot section is in a part of the substrate when the AC power supply is connected. Please note the high temperature burn.
	The power supply and the plug use the one of ratings 2A that suited the safety standard of the product according to law in country that uses it. The use of the unacceptable products causes the breakdown, generation of heat, a fire, and the electric shock.
	Please detach the AC plug from the outlet when you generate smoke, a nasty smell, an abnormal sound, and abnormal generation of heat, etc. by any chance. Using Products as it is. It causes a fire, the burn, and the electric shock.
	This product Shouldn't dismantle and remodel by the customer. It causes the breakdown, smoking, a fire, and the electric shock.
	The product is not dropped, and the strong shock is given. It causes a fire and the electric shock damaging it.
	The AC adapter cable is not t pull out of supply entered. So connecter is not pull out of supply entered. Exception: Cable can pull out of power supply. Pulling out the connector is not done with the power supply entered. It causes a fire and the electric shock damaging it.
	The connection of the cable and the interface cable is insufficient and the power supply is not turned on. It causes the breakdown, generation of heat, a fire, and the explosion.
	When moving products, cables and power supply are removed. The cable etc. is damaged, and it causes the breakdown, generation of heat, a fire, and the electric shock.

Caution

Caution	
	The power supply turning on and cutting each system follow the procedure described in the manual. It causes the breakdown of generation of heat and the equipment to occur.

General Precautions for Handling This Product

1.Circumstances not covered by product guarantee
Does not use over voltage, and use outside guaranteed temperature range.
Do not add power to the USB cable, and do not add power to the USB interface.
Do not remove or break S/N (Serial Number) sticker. These stickers are required for warranty validation.

2. Safety precautions
If used for a long time, the product may become hot (50°C to 60°C). Be careful of low temperature burns and other dangers due to the product becoming hot.
It is explained by the previous item. “1. Circumstances not covered by product guarantee”.

3. Warning
The board is selling “AS IS” .If board has Faults. You and your company acknowledge and agree risk.
Anytime, you examine New Information of this Board and Devices.
Shimafuji don’t pay the ransom that exceeds the price of the product is not paid.

CHAPTER 1. INTRODUCTION

Development Kit Board is a reference design board which is mounted a EMMA Mobile 1. This document is information for a software development, the demonstration and hardware evaluation. The Development Kit Board on EMMA Mobile 1 is embedded low power SOC. The board is including components, debug I/F, Function, system control, Connecter, Restriction and more.

1.1. Overview

The major components of the boards are described below.
CPU Board, IO board, LCD

1.1.1. CPU Board

PCB: 8 layers
Main LSI: EMMA mobile-S (μPD77630A)
Mobile DDR SDRAM: 1Gbit (8 Meg x 32 x 4 Banks)
FLASH-ROM
eMMC NAND-FLASH: 4Gbyte
IO board Interface
LCD Interface
JTAG ICE IF (Special Header; TET SICA20C20Y-GA102)
Micro SD Card IF
USB Mini AB Interface
Com Port Interface (USB mini B)
General purpose switch (2)
General purpose LED (2)
Sound interface: LINE OUT

1.1.2. IO board

PCB: 6 layers
CPU Board Interface
LCD Interface
NTSC interface: RCA Jacks
Sound interface: LINE OUT, MIC 1 Channel
Ethernet interface: RJ-45
General purpose switch matrix (14)
General purpose LED (4)
JTAG ICE IF (Mictor)
Expansion interface

1.1.3. LCD Panel

Manufacture: NEC LCD Technologies, Ltd.
Product Name: NL8048HL11-01B
Type: TFT Active matrices LCD
Size: 99.6(H) × 69.5(V) × 5.0(D) mm (typ)
Interface: FH23-51S-0.3SHW (HRS)
Touch Panel Control: SPI
Color: 16777216(8-bit digital RGB)
Pixel: 800(H) × 480(V)

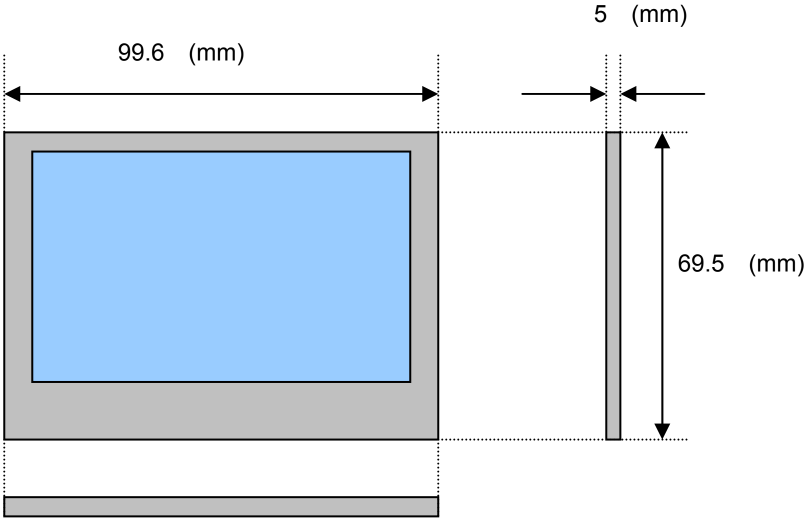


Figure 1-1 LCD Image

!	CAUTION: LCD board has bonded on PCB through Acrylic fiber board. LCD must not detach on PCB. That would cause the breakdown which cannot recover.

1.2. Connectors

1.2.1. CPU Board Image

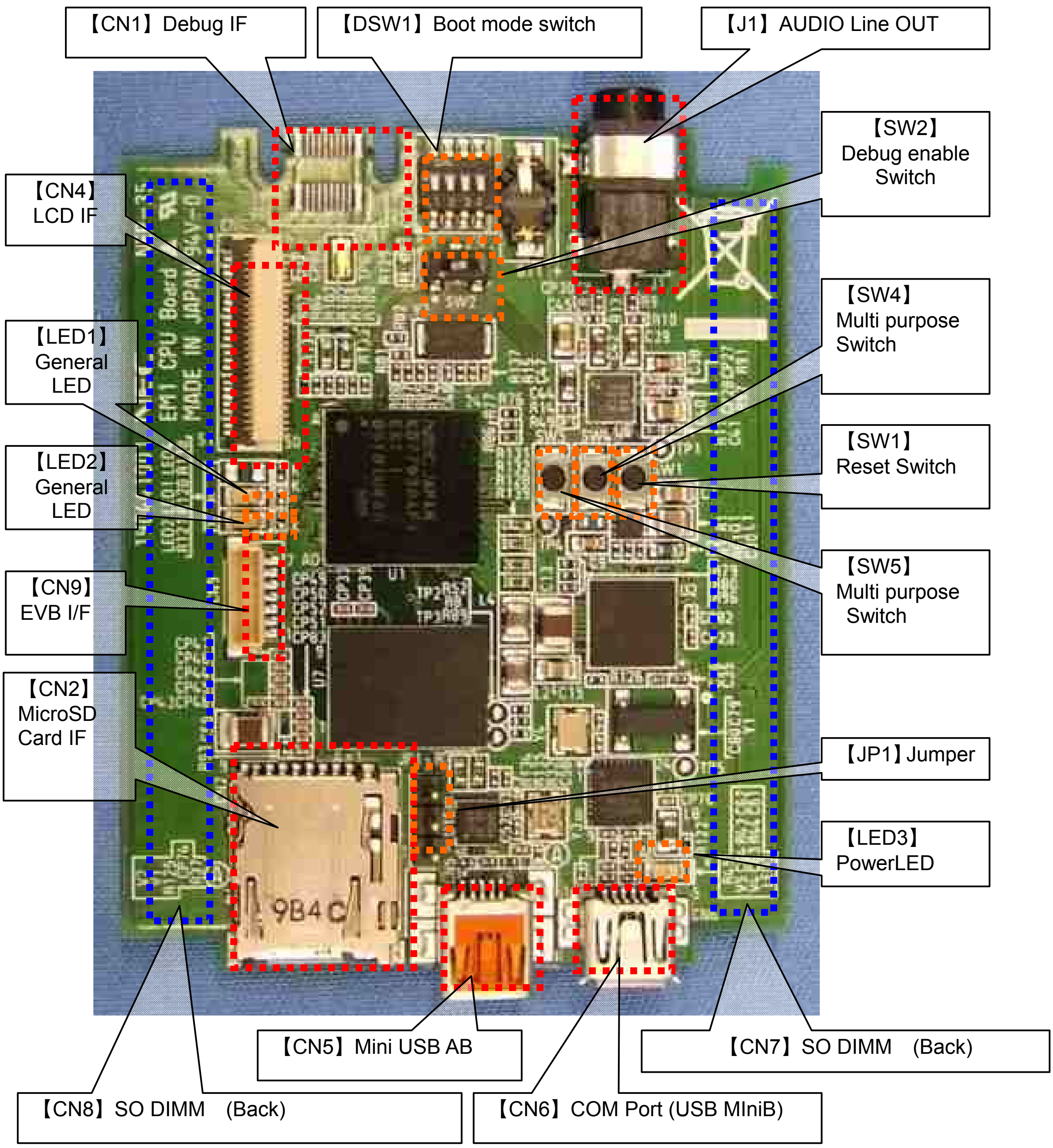


Figure 1-2 CPU Board Image

【CN1】Debug IF: Special Connecter that attached SICA20C20Y-GA102
【CN2】Micro SD Card IF
【CN4】LCD Interface
【CN5】Mini USB AB
【CN6】COM Port (USB Mini B)
【CN7】,【CN8】SO DIMM(Back)
【CN9】EVB IF
【JP1】Jumper (VBUS line switch to HOST mode/DEVICE mode)
【J1】AUDIO JACK (LINE OUT)
【DSW1】DIP Switch (Boot mode Select)
【SW1】Reset Switch (Board system reset)
【SW2】Debug Switch (Debug enable)
【SW4】【SW5】Two general purpose push Switches.

1.2.2. IO Board Image

(1) Front View

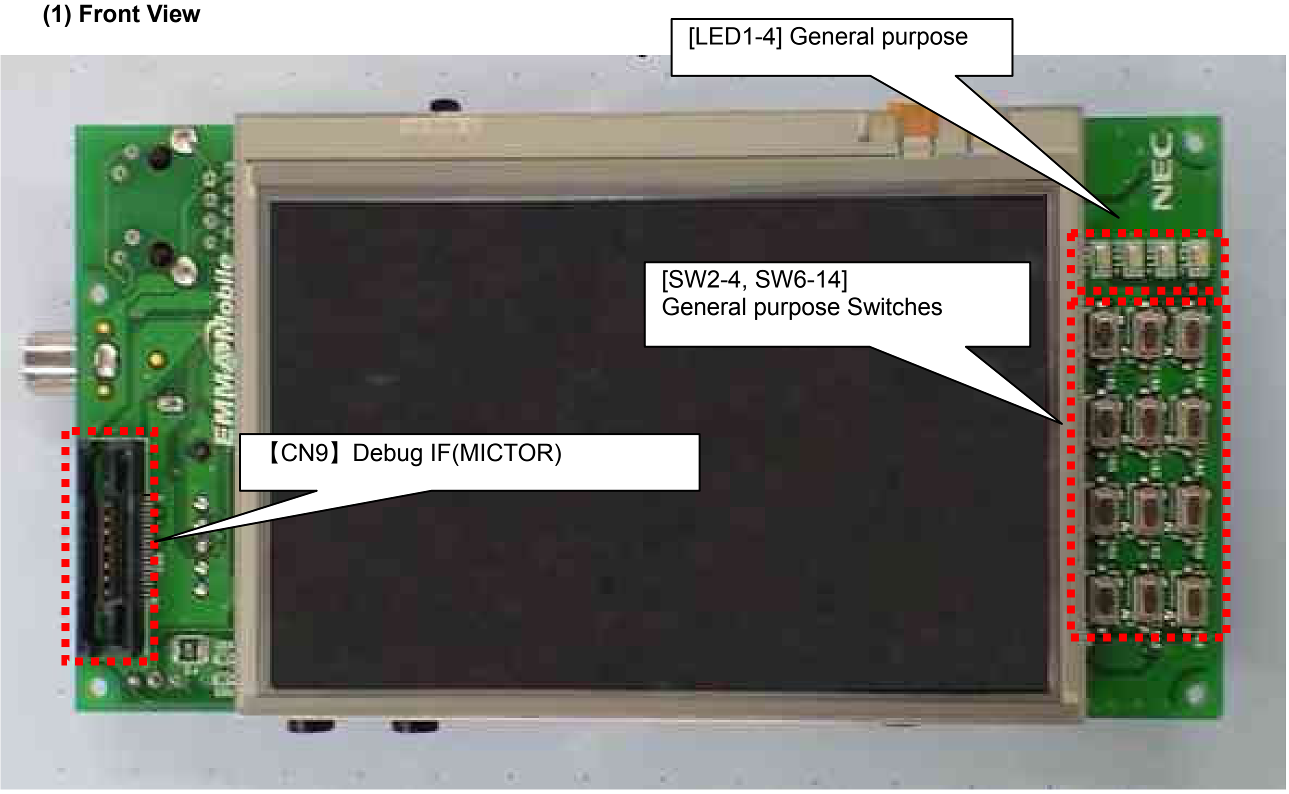


Figure 1-3 IO board Image（Front）

【CN9】Debug IF(Mictor)
【SW2-4, SW6-14】general purpose Switches
【LED1-4】general purpose LEDs

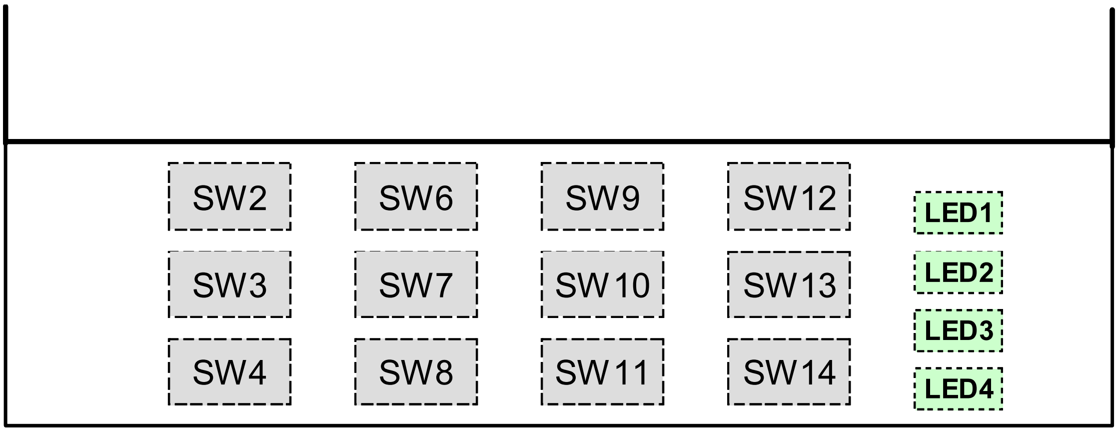


Figure 1-4 IO board Key Image（Front）

(2) Back View

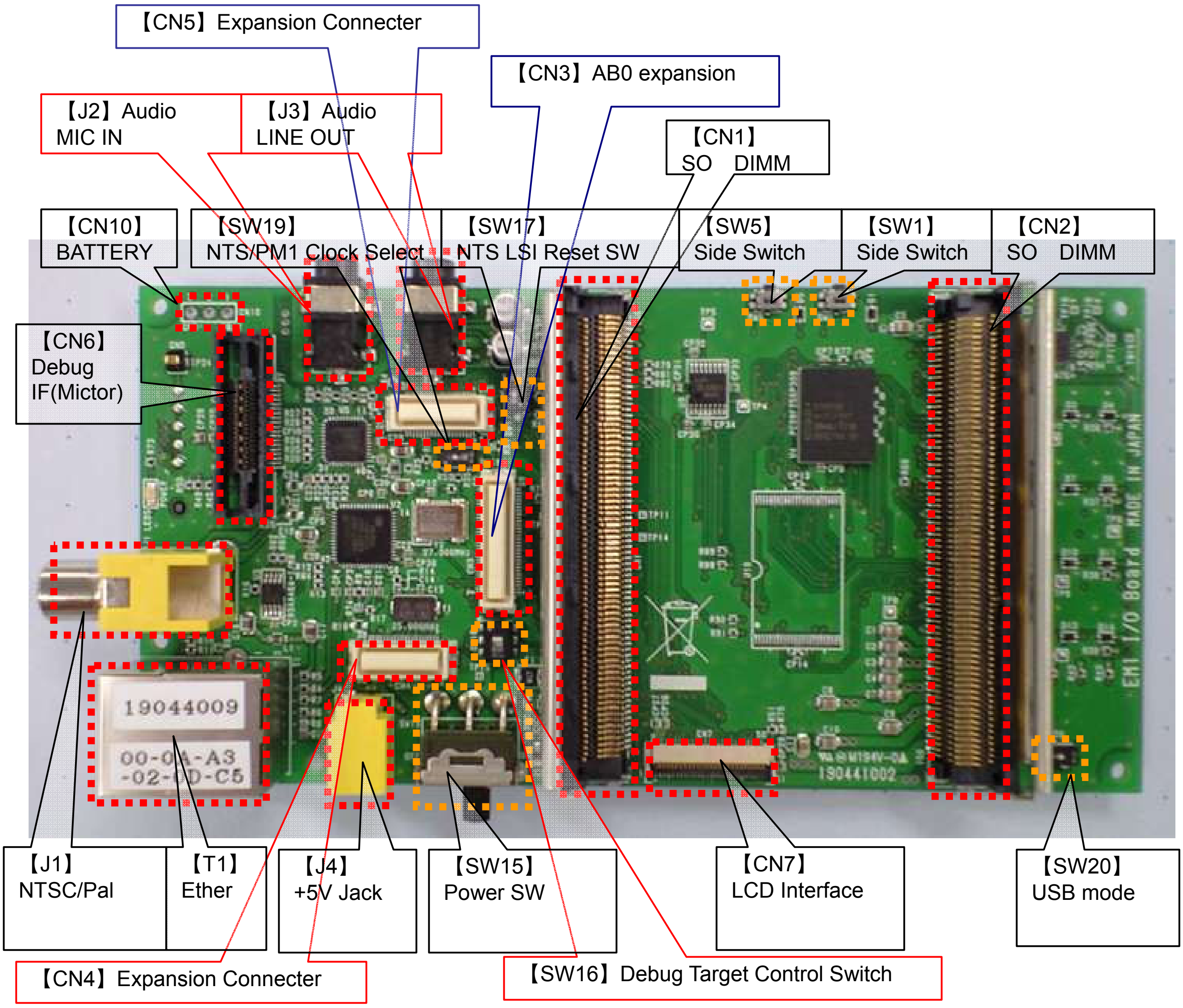


Figure 1-5 IO board Image (back)

【CN1】【CN2】CARD edge
【CN3】AB0 expansion
【CN4】【CN5】Expansion Connecter
【CN6】Debug IF(Mictor)
【CN7】LCD Interface
<R> 【CN10】BATTERY Connecter
【SW1】【SW5】Side Switch(x2)
【SW15】Power Switch
【SW16】Debug target Control switch (CPU or DSP)
【SW17】NTS LSI Reset SW
【SW19】NTS/PM1 Clock Select
【SW20】use for USB mode switch connected to EM1-GIO_P01.
【J1】NTSC/Pal Output
【J2】AUDIO JACK (MIC IN)
【J3】AUDIO JACK (LINE OUT)

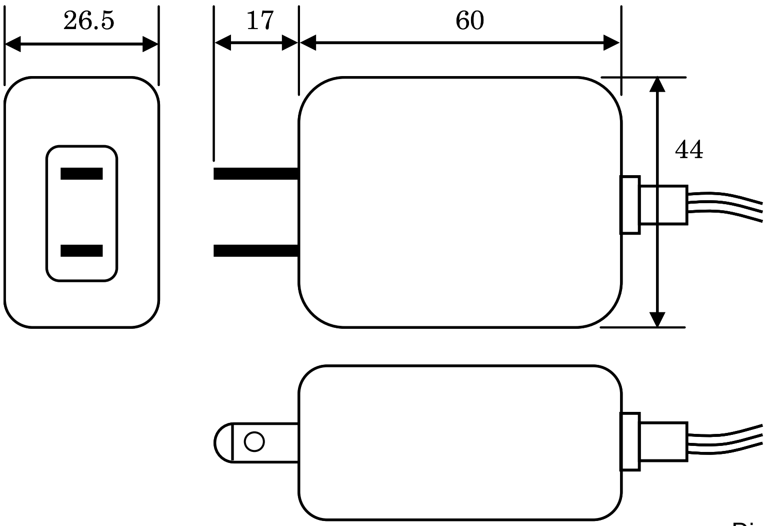
1.3. Power Supply

CAUTION:
The travel adapter is not recommended for AC/DC adapter use.
And should isolate from water and dust.

Switching AC/DC Adapter

Manufacture: UNIFIVE
Product Name: US300520
INPUT : AC100V-120V, AC100V-240V, 50/60Hz
OUTPUT : 5V,2A
SAFETY : PSE-MARK,UL/CUL,CE,CB,BSMI
DIMENSION: L×W×H: 60×44×26.5 [mm]
Plug Type: 2 pin, IEC Technical Report 60083, JIS C 8303

(1) Input Side



Dimension is [mm].

(2) Output Side

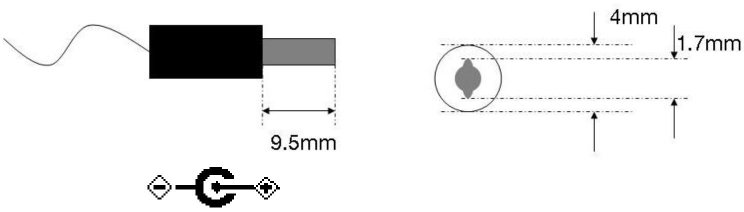


Figure 1-6 AC/DC Adapter Image

CAUTION:
If you need to prepare other AC/DC adapter for un-match AC plug, your domestic regulation and so on, please must buy same mechanical specification and feeder specification regarding DC side. Those are EIAJ2 and OUTPUT: 5V-2A.

1.4. Development Tools Connection

1.4.1. CPU Board ICE Interface [CN1]

Special Header; TET SICA20C20Y-GA102
Header; ARM 20Pin

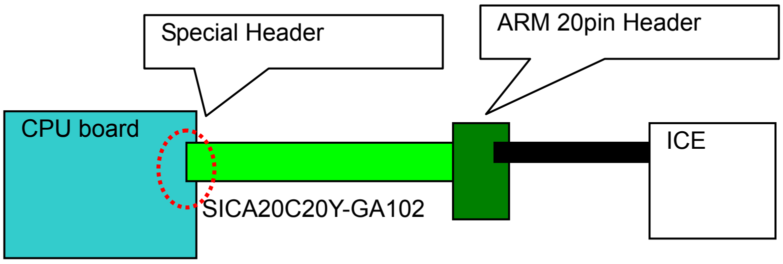


Figure 1-7 CPU Board ICE Interface

TETC
Tokyo Eletech Corporation
3-10 Akihabara, Taito-ku, Tokyo, 110-0006, Japan
Mail e-components@tetc.co.jp
TEL +81-(0)3-5295-1661
FAX +81-(0)3-5295-1775
Web http://www.tetc.co.jp/e_enquete.htm
On Apr.2009

You can get information of "TETC SICA20C20Y-GA102" on TETC web page.
Please confirm that when you need a interface connector cable of "TETC SICA20C20Y-GA102" to ICE.

1.4.2. IO board Debug Interface [CN6], [CN9]

Debug interface is used 38 Mictor connector.
The interface is not included ETM trace signal as below pin assignment.

Header: Mictor connector

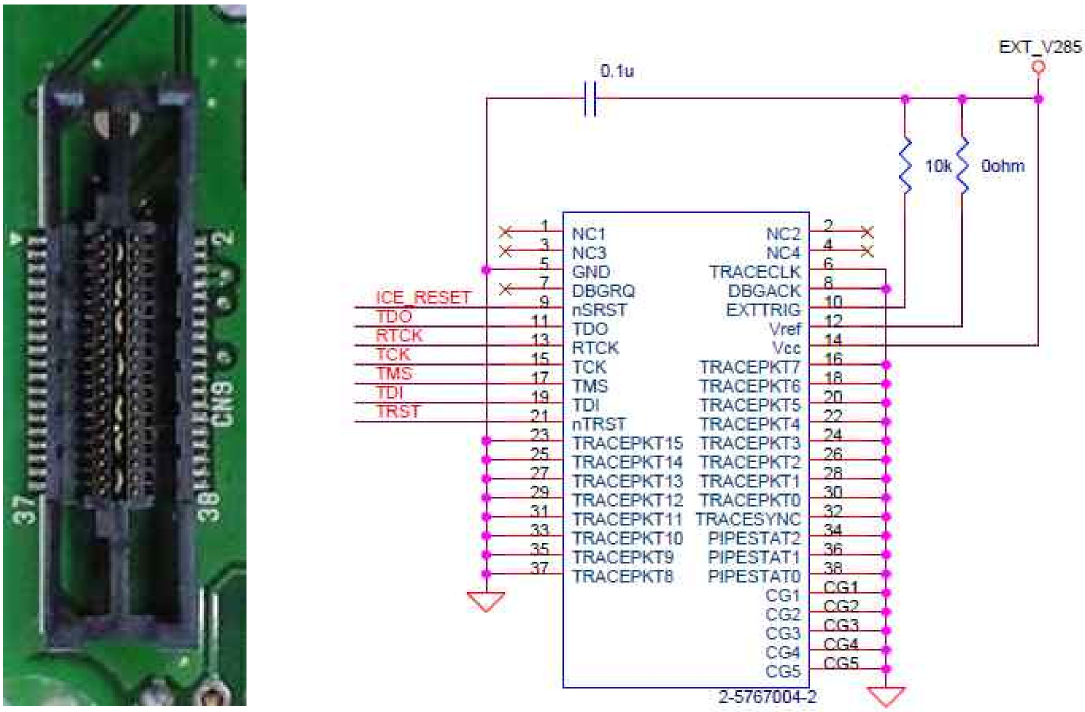


Figure 1-8 Debug Interface [CN6], [CN9]

CHAPTER 2. FUNCTIONS

2.1. Board Function Summary

Table 2-1 Board Function

Items		Contents
Board Structure		CPU Board + IO Board 、CPU Board works independently
CPU		EM1-S
Power LSI		Dialog DA9052
Memory	**CPU Board**	MobileDDR 1Gbit（128Mbyte） eMMC NAND ４GByte
	IO Board	NOR Flash 256Mbit（32Mbyte） Nand Flash (not mounted） 4Gbyte
Interfaces	**CPU Board**	LCD Direct Connect IF Audio IF : Audio mini Jack - Line Out x1 USB IF: miniAB Connector x1. MicroSD Card Slot x1 Debug I/F : mini JTAG IF(Special) - for ARM Only USB IF for Console: miniB Connector x1 – Console IF (COM-Port)
	IO Board	LCD （WVGA Size, Supports Touch Screen、Back light), Audio IF: Audio mini Jack – MIC In x1, Line Out x1 TV Out（NTSC/PAL）, LAN I/F(RJ45), Debug I/F mictor type connector x1 General purpose Connector (for WLAN/BT/DTV/Camera Module）, ASYNC Expansion Connector x1、 CPU Board – IO Board Connector （EM Connector）
Button SW LED etc.	**CPU Board**	Switch x2, LEDs x 2 (for General purpose）, Power LEDx1, Dip Switch(Boot mode select, Debug enable) , USB VBUS route select (Jumper)
	IO Board	Key switch（3x4 LCD side、side switch x2) LEDs for General purpose x4、 Dip SW(ARM/DSP ICE selection)
Power	**Power Source**	DC Power supply +5V-2A (EIAJ2) Li-Ion Battery (Connector Only) USB VBUS power supply
	Charge function	Supports Li-Ion battery Charge by DC Power supply or USB VBUS
<R> **Size**		Case: 154 x 88 x 32mm approx. CPU Board PCB: 55.6 x 70.0 mm typ. IO Board PCB: 140.0 x 70.0 mm typ.
Quality Specs	**Standards Support**	RoHS（EU) Support AC adapter: Electrical Appliance and Material Safety Law Support (PSE-MARK,UL/CUL,CE,CB,BSMI)

2.2. Parts Detail Descriptions

2.2.1. EMMA Mobile1-S (CPU LSI)

The EMMA Mobile1 is a multimedia processor for mobile applications and low power applications that integrates a logic chip incorporating a CPU and DSP in one package.

・CPU: ARM1176JZF-S (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
・DSP: SPXK701 (Max. 500 MHz, I-cache: 32 KB, D-cache: 32 KB)
・DMA controller
・Image processing
  Image processor (resizing, filtering, etc.)
  Image rotator (0□, 90□, 180□, 270)
  Graphics DMA (ROP and FILL)
  Image composer (LCD output image synthesis)
・H.264/MPEG-4 AVC accelerator
・Peripheral interfaces
  Memory interface: External bus interface (16 bits: Flash memory, etc.), NAND interface
  Serial interfaces: UART, I2C, audio/voice, SPI, IrDA
  SD card interface (with SDIO)
  Image-related interfaces: LCD interface, terrestrial digital TV interface (DTV)
  ITU-R.BT656 interface (NTS)
  General-purpose I/O interface
  ULPI interface
・Package(481-pin fine-pitch BGA package (12.7x12.7 mm))

2.2.2. Power LSI (DA9052)

The DA9052 is a highly integrated PMIC subsystem with supply domain flexibility to support a wide range of application processors, associated peripherals and user interface functions

・Switched DC/USB Charger with power path management
・4 Buck Converters (3 have DVS) 0.5V – 3.6V up to 1Amp
・10 Programmable LDO’s High PSRR, 1% accuracy
・Low power Backup Charger 1.1 – 3.1V up to 6mA
・32kHz RTC Oscillator
・General Purpose ADC with touch screen interface
・High voltage white LED driver 24V / 50mA Boost, 3 strings
・16bit GPIO bus for enhanced
・Wake up and peripheral control
・Dual serial control interfaces
・Unique USB supply detection and charge current selection
・Unique ID code capability via OTP memory
・Package(86LD UFNBA-QFN (7x7 mm))

2.2.3. DDR-SDRAM (MT46H32M32LFCM-6)

The MTH32M32LFCM-6 Mobile is a Low-Power DDR SDRAM

・Cycle time (6 ns)
・32 Meg x 32 (8 Meg x 32 x 4 banks)
・Package(90-Ball VFBGA 10 x 13mm)

2.2.4. EMMC NAND Memory (MTFC4GDKDI-ET or KMCEG0000A)

EMMC NAND Memory is used as next two options on the board. And that is different by board revision. The board information can be confirmed by 5.5 Board Revision and 5.6 Board Information in EEPROM. Please refer to eMMC bit of EEPROM Address's 0x10 for the revision recognizing of software view point.

The KMCEG0000A is a NAND Flash Memory and MMC in one package.
・Simple read/write memory using industry-standard MMC protocol 4.2 interface
・Common solution for embedded and external flash memory
・4G Byte Flash Memory
・Package(153-Ball FBGA 11.5x13mm)
・Low-cost embedded solution with MLC NAND
・Performance increase costs less
・Dual power supply
  3.0V (2.7V ~ 3.3V) for MLC NAND Flash
  1.8V/3.0V for I/O
・MMC4.1 or 4.2 interface
  x1, x4, x8 bus & 26MHz, 52MHz

The MTFC4GDKDI is a NAND Flash Memory and MMC in one package.
・Isolated Multimedia Card (MMC) interface
・4G Byte Flash Memory
・Package(169-Ball FBGA 12 x 16mm)
(MMC Specification)
・MMC system specification version 4.2 MMC-mode-protocol-compliant
・Advanced 10-signal interface
・ x1, x4, and x8 I/Os, selectable by host
・MMC mode operation
・Command classes
  Class0 (basic) Class 2 (block read) Class 4 (block write) Class 5 (erase) Class 6 (WRITE protection) Class 7 (lock card)
・MMCplus™ and MMCmobile™ protocols
・Password protection
・Permanent and temporary write protect
・Supports basic file formats
・52 MHz clock speed (MAX)
・416 Mb/s data rate (MAX)
・Fully backward-compatible with previous MMC modes
・ECC and block management implemented

2.2.5. NOR Flash Memory (PC28F256P30B85)

The PC28F256P30B85 is NumonyxTM StrataFlash® Embedded Memory(256MBit)
・100 ns initial access
・25 ns 16-word asynchronous-page read mode
・52 MHz with zero WAIT states
・Buffered Enhanced Factory Programming (BEFP) at 2.0 MByte/s (Typ) using 512-word buffer
  □1.8 V buffered programming at 1.5MByte/s
・Package(64-Ball Easy BGA 10 x 13mm)

2.2.6. Ether (LAN9221)

The LAN9221 is a Highly-performance 16bit Non-PCI 10/100 Ethernet Controller
・Host bus interface (16bit data bus)
・1.8V to 3.3V variable voltage I/O accommodates wide range of I/O signaling
・Integrated PHY with HP Auto-MDIX support
・Integrated checksum offload engine helps reduce CPU load
・Package(56-QFN 8 x 8mm)
・EEPROM interface for MAC address storage. LAN9221 can load the MAC address automatically after reset.

2.2.7. USB-PHY (ISP1504 or USB3329)

USB PHY is used as next two options on the board. And the USB phy is different by board revision. The board information can be confirmed by 6.3 Board Revision and 6.4 Board Information in EEPROM. Please refer to USB-PHY bit of EEPROM Address's 0x10 for the revision recognizing of software view point.

The ISP1504 is USB 2.0 Transceiver as below:

・Universal Serial Bus Specification Rev. 2.0
・On-The-Go Supplement to the USB 2.0 Specification Rev. 1.2
・UTMI+ Low Pin Interface (ULPI) Specification Rev 1.1
・Interfaces to host, peripheral and OTG device cores; optimized for portable devices or system ASICs with built-in USB OTG device core
・Complete Hi-Speed USB physical front-end solution that supports high-speed(480 Mbit/s), full-speed (12 M bit/s) and low-speed (1.5 M bit/s)
・Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
・Highly optimized ULPI-compliant interface
(60 MHz, 8-bit interface between the core and the transceiver)
・Package(36balls TFBGA 3.5 x 3.5mm)

The USB3329 is USB 2.0 Transceiver as below:

・Highly integrated, Hi-Speed USB 2.0 transceivers
・Integrated VBus over-voltage protection (up to +30V)
・Integrated USB switch
・Internal ESD protection circuits
No external ESD protection circuits required
・Integrated 3.3V LDO regulator
・Ability to use the USB connector as single port of connection
・Switch Hi-Speed data, battery charging, and stereo/mono audio accessories
・UART mode
・Variable I/O voltage capability
・Low power and standby modes of operation to minimize power consumption
・Low jitter PLL makes it possible to accept "noisy" clock sources
・Supports commercial (0° to 70° C) and industrial (-40° to 85° C) temperature ranges

2.2.8. COM-Port (FT232RQ)

The FT232RQ is a USB to serial UART interface
・Single chip USB to asynchronous serial data transfer interface.
・Entire USB protocol handled on the chip. No USB specific firmware programming required.
・Fully integrated 1024 bit EEPROM storing device descriptors and CBUS I/O configuration.
・Supports bus powered, self powered and high-power
・bus powered USB configurations.
・UART signal inversion option.
・UHCI/OHCI/EHCI host controller compatible.
・USB 2.0 Full Speed compatible.
・Package(32pin QFN 5 x 5mm)

2.2.9. TV-OUT (ADV7179KCPZ)

The ADV7179 is a Video Encoder transfer to PAL/NTSC from ITU-R1 BT601/BT656 YCrCb
・10bit video DAC
・Multi standard video output (CVBS Y/C)
・Video input data port(CCIR-656 4：2：2、8bit parallel format)
・Composite, S video simultaneous output or RGB (SCART)/YUV video output can be set.
・2-wire MPU serial interface(I2C® interchangeability and Fast I2C)
・Package(40 pin LFCSP 6x 6mm)

2.2.10. Audio LSI (AK4648EC)

The AK4648 is a stereo CODEC with a built-in Microphone-Amplifier, Headphone-Amplifier and Speaker-Amplifier.

・Recording Function
  (4 Stereo Inputs Selector, Stereo MIC Input (Full-differential or Single-ended), Stereo Line Input,
  MIC Amplifier, Digital ALC (Automatic Level Control), Wind-noise Reduction Filter,
  Stereo Separation Emphasis, Programmable EQ)
・Playback Function
  (Digital De-emphasis Filter, 5-Band Equalizer, Soft Mute, Digital Volume,
  Digital ALC (Automatic Level Control), Stereo Separation Emphasis, Programmable EQ,
  Stereo Line Output, Stereo Headphone-Amp, Stereo Speaker-Amp, Analog Mixing: 4 Stereo Input)
・µP I/F: I2C Bus (Ver. 1.0, 400 kHz Fast-Mode)
・Master/Slave mode
・ Audio Interface Format: MSB First, 2's complement
  (ADC: 16bit MSB justified, I2S, DSP Mode,
  DAC: 16bit MSB justified, 16bit LSB justified, 16-24bit I2S, DSP Mode)
・Package: (CSP 3.7mm x 3.8mm)

2.2.11. NAND Flash Memory (K9F1G08U0A) NOT MOUNTED on the board.

The K9F1G08U0A is a 128M x 8 Bit / 256M x 8 Bit NAND Flash Memory
・Memory Cell Array : (128M + 4,096K)bit x 8bit
  Data Register: (2K + 64) bit x8bit Cache Register: (2K + 64) bit x8bit
・Automatic Program and Erase
  Page Program : (2K + 64)Byte Block Erase : (128K + 4K)Byte
・Page Read Operation
  Page Size: 2K-Byte Random Read: 25µs (Max.)
  Serial Access: 30ns (Min.) -3.3v device 50ns (Min.) -1.8v device
・Fast Write Cycle Time Program time : 200µs(Typ.) Block Erase Time : 2ms(Typ.)
・Command/Address/Data Multiplexed I/O Port
・Package(48-pin TSOP 12x20mm)System Control

3.1. System Block Diagram

<R>

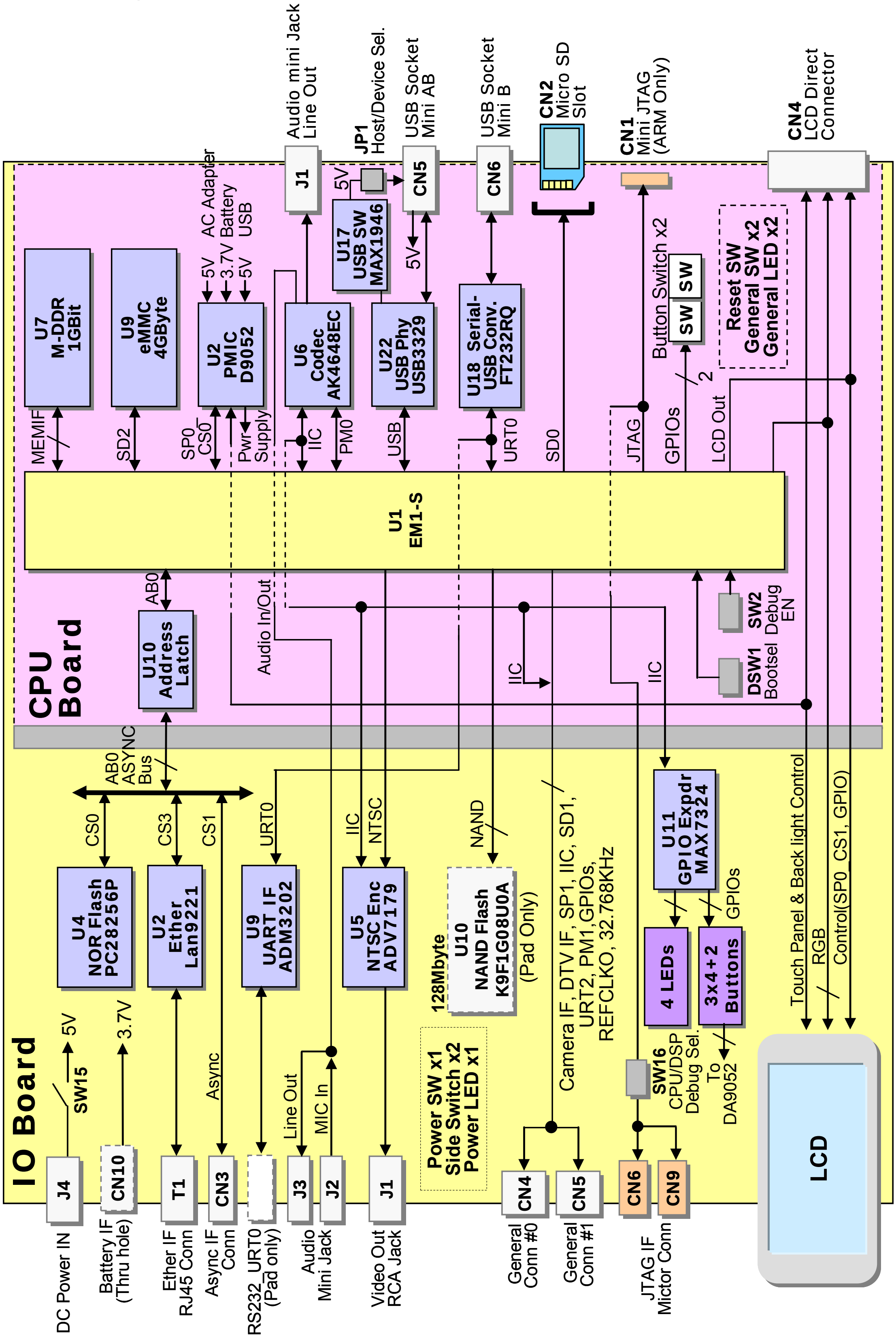


Figure 3-1 System Block Diagram

3.2. Memory Map

3.2.1. All Memory Bank

Address	BANK	Description	Target Module
0000_0000H – 0FFF_FFFFH	BANK 0	NOR FLASH	AB0
1000_0000H – 1FFF_FFFFH	BANK 1	NOR FLASH EXTERNAL Device	AB0
2000_0000H – 2FFF_FFFFH	BANK 2	EXTERNAL Device	AB0
3000_0000H – 3FFF_FFFFH	BANK 3	DRAM	MEMC
4000_0000H – 4FFF_FFFFH	BANK 4	APB Bus #0	PB0
5000_0000H – 5FFF_FFFFH	BANK 5	Async Bus #1	AB1
6000_0000H – 6FFF_FFFFH	BANK 6	AHB Slave	SWL1
7000_0000H – 7FFF_FFFFH	BANK 7	Reserved	
8000_0000H – 8FFF_FFFFH	BANK 8	Reserved	
9000_0000H – 9FFF_FFFFH	BANK 9	Reserved	
A000_0000H – AFFF_FFFFH	BANK 10	Internal SRAM	SRC
B000_0000H – BFFF_FFFFH	BANK 11	Reserved	
C000_0000H – CFFF_FFFFH	BANK 12	APB1	PB1 (PMU)
D000_0000H – DFFF_FFFFH	BANK 13	Reserved	
E000_0000H – EFFF_FFFFH	BANK 14	Reserved	
F000_0000H – FFFF_FFFFH	BANK 15	Boot ROM	AXL1

Figure 3-2 EMMA Mobile1 ALL Memory Bank

3.2.2. BANK 0/1/2

BANK 0/1/2: AB0 (NOR FLASH/External Device)
NOR (0000_0000H - 01FF_FFFFH)
Ether (2000_0000H - 20FF_FFFFH) example mapping

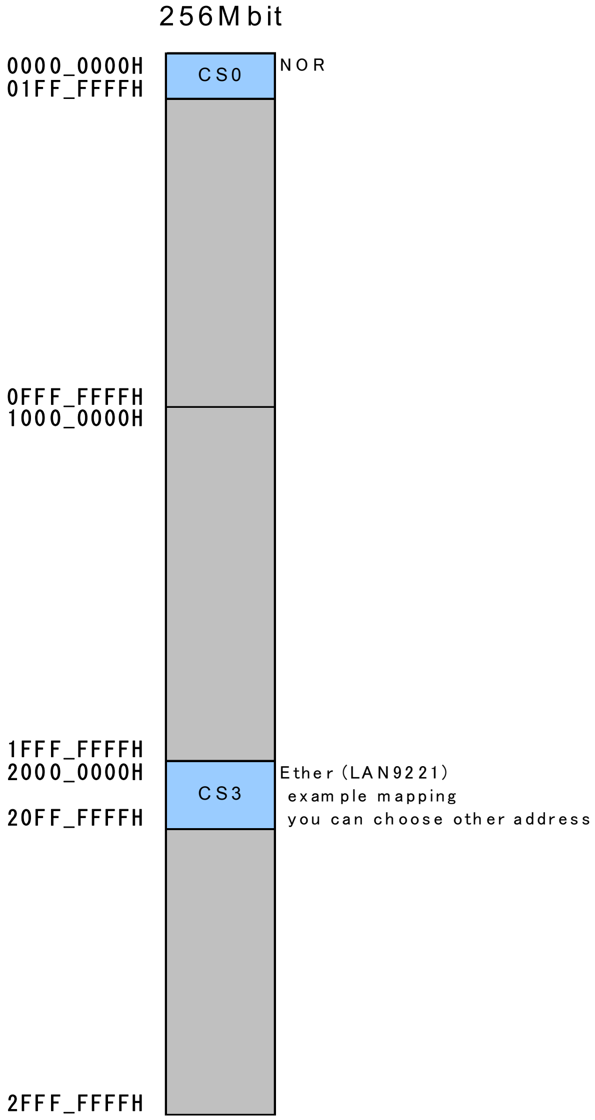


Figure 3-3 EMMA Mobile1 NOR and Asynchronous Bus0 (No.0) Memory Map

3.2.3. BANK3 DRAM AREA

BANK 3: MEMC(DRAM) (3000_0000H - 37FF_FFFFH)

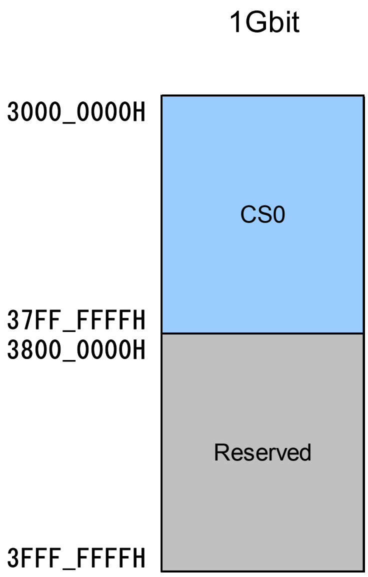


Figure 3-4 EMMA Mobile1 DRAM Memory Map

3.3. Power System

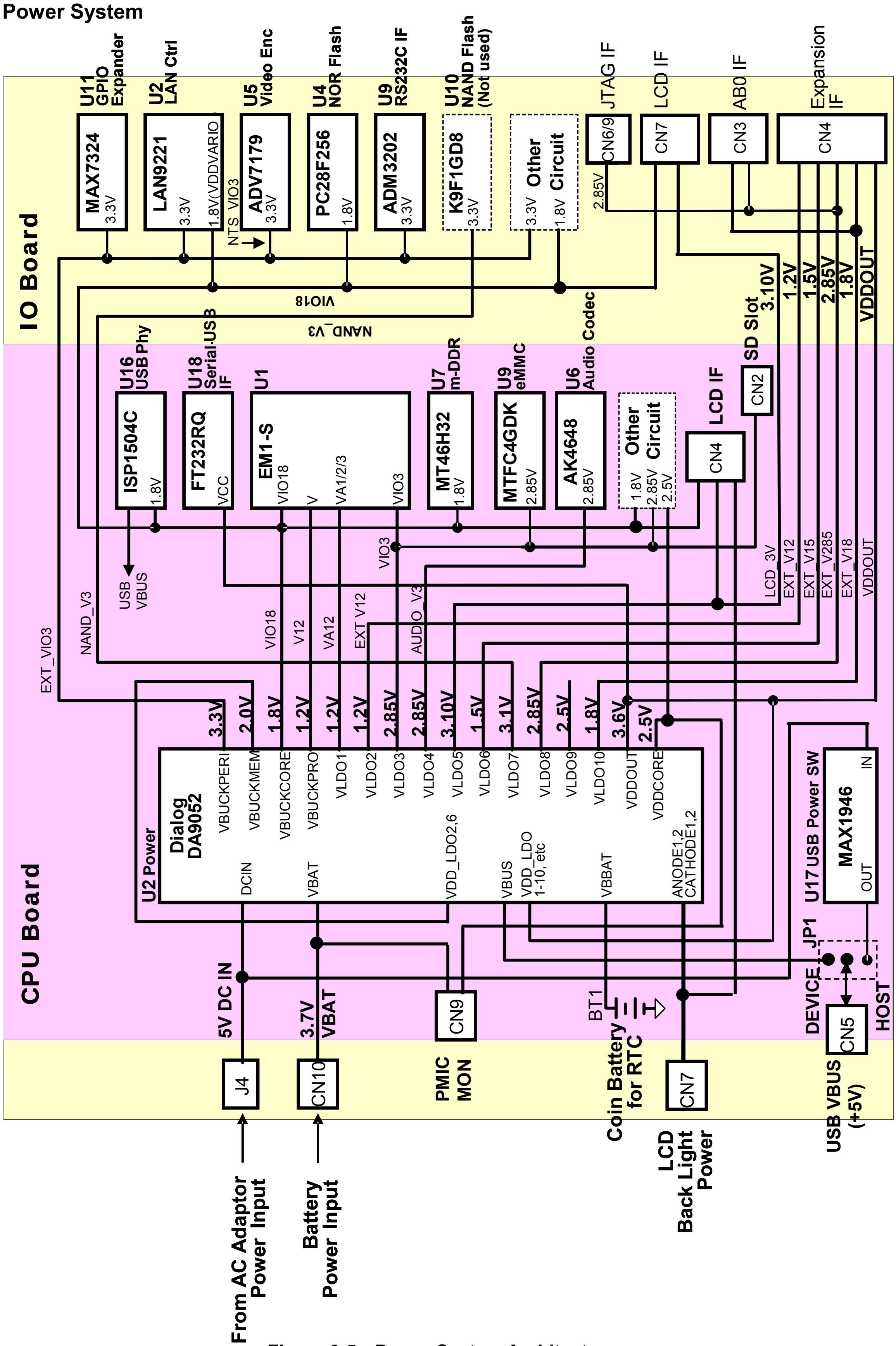


Figure 3-5 Power System Architecture

3.3.1. Power System Configuration

Table 3-1 Power System Configuration

No	Power LSI Source	Power line Symbol	Input Source	Max Current	Set Voltage	Other LSI of CPU Board	Other LSI of IO Board
1	VBUCKPERI	EXT_VIO3	VDDOUT	500mA	3.3V	ISP1504:PSW_N line	LAN9221-VDD33(3.3V+/-300mV) 133mA ADV7179：NTSC(3.0-3.6V) 155mA ADM3202: RS232C Other Circuits（Key, LED, LAN IF Circuit）
2	VBUCKMEM	VBUCKMEM	VDDOUT	500mA	2.0V	DA9052 Return	NC
3	VBUCKCORE	VIO18	VDDOUT	700mA	1.8V	EM1S / VIO18 MDDR(1.7V) ：70mA ISP1504C： Vcc:3.0~4.0V, 48mA typ Other Circuits	LAN9221-IO(1.8V+/-10%) 7mA PC28F256: NOR Flash Other Circuits
4	VBUCKPRO	V12	VDDOUT	700mA	1.2V	EM1S / V：700mA	NC
5	LDO1	VA12	VBUCKMEM	40mA	1.2V	EM1S / V1, V2, V3	NC
6	LDO2	EXT_V12	VBUCKMEM	100mA	1.2V	NC	Expansion Connector 1.2V –CN4 AB0 Connector – CN3
7	LDO3	VIO3	VDDOUT	200mA	2.85V	eMMC(2.7-3.6V) 85mA typ SD Slot VDD EM1S / VIO3 ：100mA Other Circuits	NC
8	LDO4	AUDIO_V3	VDDOUT	150mA	2.85V	AK4648(2.6-3.6V) 25mA	
9	LDO5	LCD_3V	VDDOUT	100mA	3.1V	LCD(3.10V) 70mA – CN4	LCD(3.10V)：70mA – CN7
10	LDO6	EXT_V15	VBUCKMEM	150mA	1.5V	NC	Expansion Connector 1.5V –CN4 AB0 Connector – CN3
11	LDO7	NAND_V3	VDDOUT	200mA	2.85V	NC	K9F1G08（NAND Flash）
12	LDO8	EXT_V285	VDDOUT	200mA	2.85V	NC	Expansion Connector 2.85V –CN4 AB0 Connector – CN3 ICE Connector – CN6, CN9
13	LDO9	TSREF	VDDOUT	100mA	2.5V	NC	NC
14	LDO10	EXT_V18	VDDOUT	250mA	1.8V	NC	Expansion Connector 1.8V –CN4 AB0 Connector – CN3
15	VDDOUT	VDDOUT	DC IN or VBAT or VBUS	-	3.6V	DA9052 Power Circuits FT232RQ(USB)： Vcc: 4.0-5.25V, 15mA typ	Expansion Connector VDDOUT – CN4
16	VDDCORE	VDDCORE	-	-	2.5V	DA9052-ERR_RST_REQB OTP IF – CN9	NC

3.3.2. EM1-DA9052 Connection

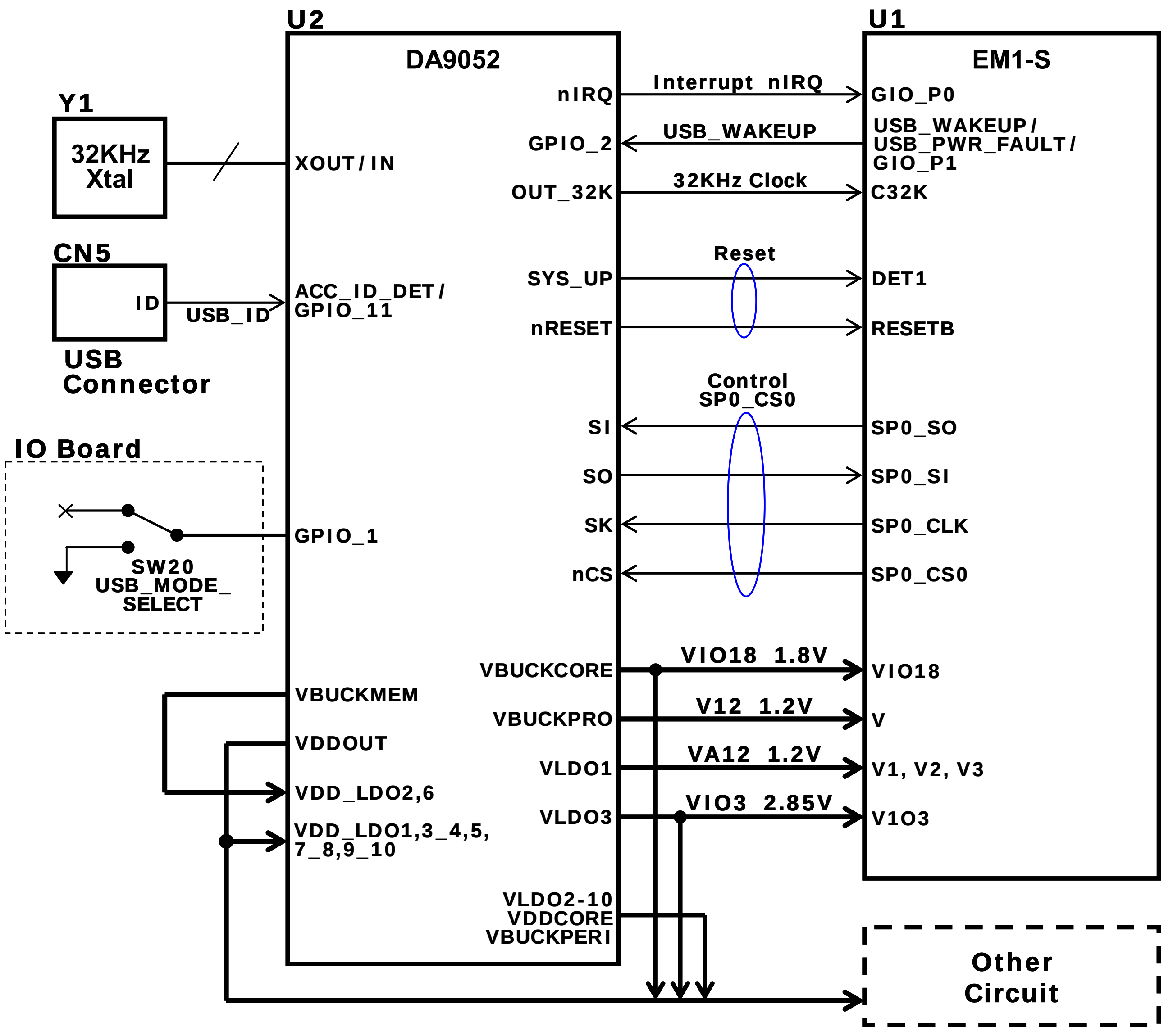


Figure 3-6 DA9052 – EM1 Connection

3.3.3. Power down Control for Board device.

Table 3-2 Power down control for board devices

Device Type	Name	Explanation
CPU & Power LSI	**EM1-S**	Combination of EM1-S and DA9052 is able to realize various power down modes. For detail Information: EMMA Mobile1-S Data Sheet and User's Manual and DA9052 Data Sheet.
Mobile DDR	**MT46H32M32LF**	This device has DPD (Deep-Power down) mode. When EM1-S send DPD command to MT46H32M32LF by way of memory interface, the device enters to DPD mode. For detail information, Please see MT46H32M32LF data sheet.
eMMC	**MTFC4GDKDI**	(No power down mode)
Audio Codec	**AK4648EC**	**- Power source for AK4648 is separated from other power source (Audio_V3). This power source line is controllable independently.** **- Users can set AK4648 to power down mode by GPIO control** Set GIO_P9 to low : PDN pin of AK4648 will be activated and AK4648 will be set into power down mode. **- For detail information, Please see AK4648 Data Sheet.**
USB Phy	**ISP1504C**	**Users can set AK4648 to power down mode by GPIO control:** -Set GIO_P47 to High: CS_N/PWRDN pin of AK4648 will be activated and ISP1504C will be set into power down mode. **For detail information, Please see ISP1504C Data Sheet.**
USB-Serial Converter	**FT232RQ**	**(No power down mode)**
NOR Flash	**PC28F256P30B85**	**(No power down mode)**
Video Encoder	**ADV7179**	**Users can reset ADV7179 when this device does not be used,** - Set SW17 "off" of IO Board Off - Set SW17 "on" of IO Board and GIO_P8 set to reset (Low). **For Detail Information, Please see ADV7179 Data Sheet.**
LAN Controller	**LAN9221**	**Users can reset LAN9221 by GPIO control** - Set GIO_P44 set to reset(Low) **For Detail Information, Please see LAN9221 Data Sheet.**
NAND Flash	**K9F1G08U0A**	**(No power down mode)**
Other Devices	**-**	

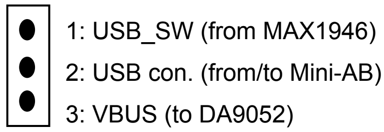
3.3.4. Power Supply Source

Design Kit Board has two options about power supply source.
The supply source is selected by JP1 physically. And SW20 on IO Board should set to find the status for software point of view. Please also refer to 4.1.8 JUMPER [JP1] about JP1 and Table 3-15 IO Board Switches and LEDs (2) about SW20.

Table 3-3 CPU Board JUMPER [JP1]

SET	Setting
1-2	USB(HOST MODE)
2-3	USB(DEVICE MODE)

[JP1]



(1) USE CASE1: VBUS power supply
USB VBUS power supply can drive CPU board only.
(USB VBUS power cannot drive CPU board and IO board configuration.)
JP1 2-3 must be shorted.

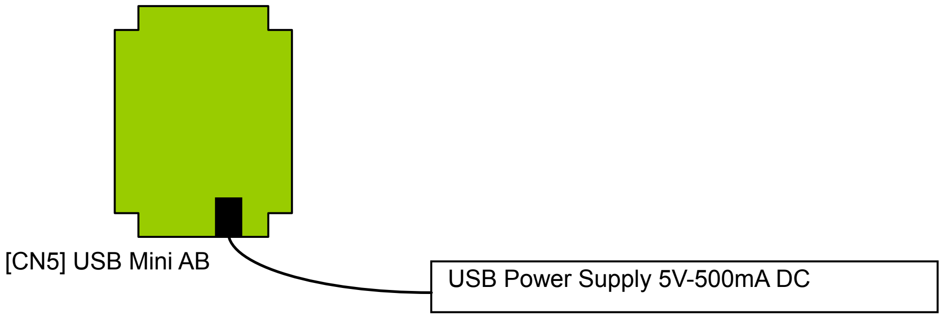


Figure 3-7 CPU Board

(2) USE CASE2: AC adapter power supply
CPU Board and I/O Board configuration is supplied by AC adapter.

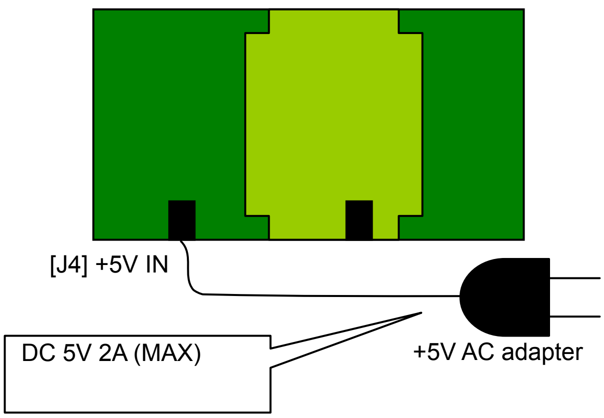


Figure 3-8 CPU Board and I/O Board

3.3.5. RTC Backup Battery

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One coin battery is mounted on the board for power source of the RTC in DA9052. This coin battery is ML414, capacity is 1.2mAh. When the AC adapter or the Lithium ion battery is connected to this board, coin battery charge starts automatically.

ML414 is Rechargeable Li-ion battery. The battery must avoid using till fully low voltage. When the Development Kit Board is not used during long time, please detach the coin battery.

Please remove the battery when the coin battery performance has deteriorated.

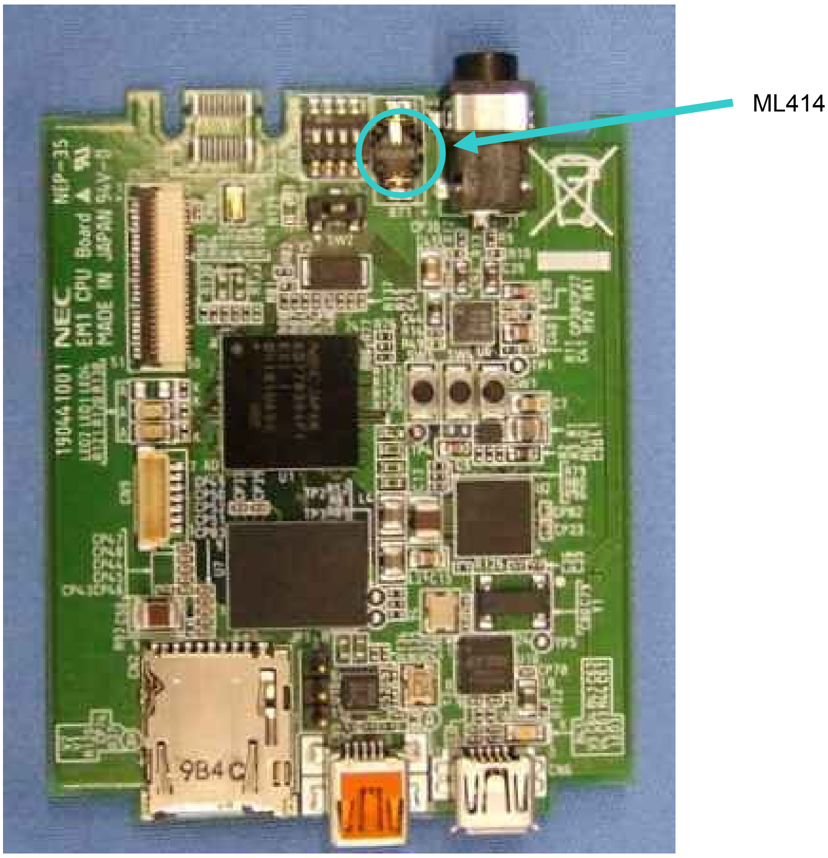


Figure 3-9 Position of ML414

3.4. Clock System

3.4.1. CPU Board Clock Tree Structure

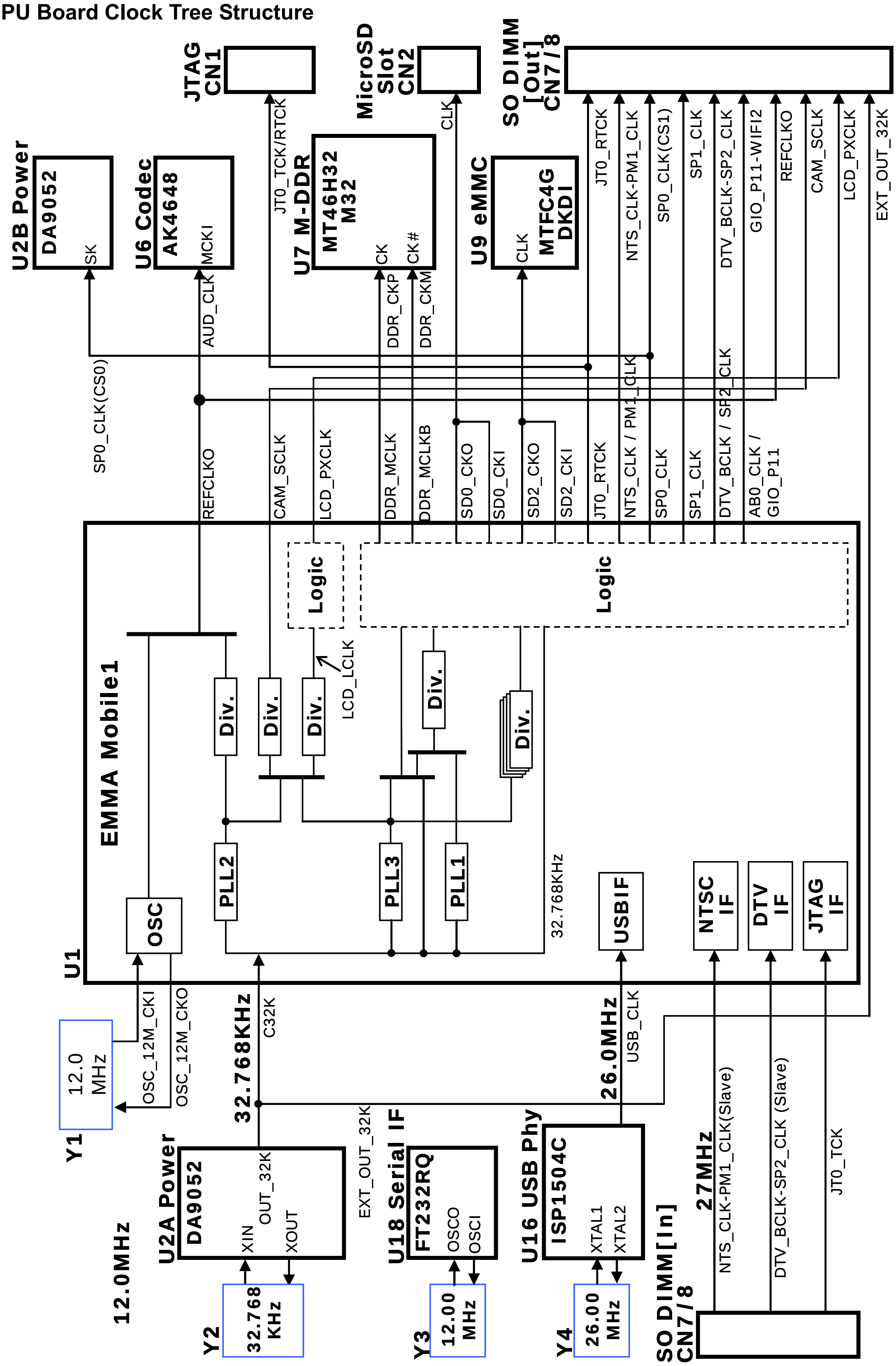


Figure 3-10 Clock Source on CPU Board

3.4.2. IO Board Clock Tree Structure

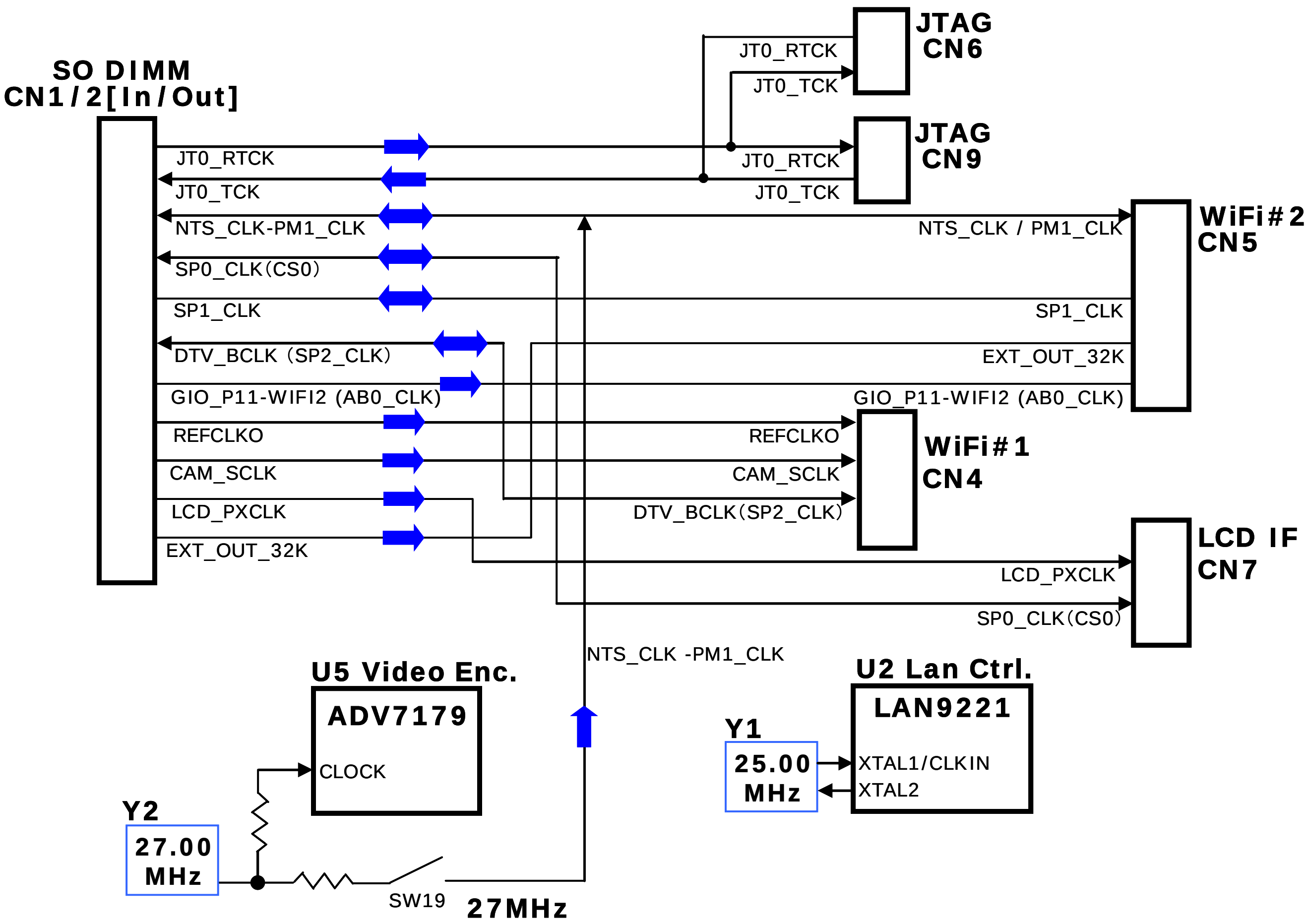


Figure 3-11 Clock Source on IO Board

- Nand Flash: Clock Signal Source corresponds to WE/RE Signal.
- NOR Flash: Clock Signal Source corresponds to AB WR/RD Signal.

3.5. Reset System

3.5.1. Reset System Architecture

<R>

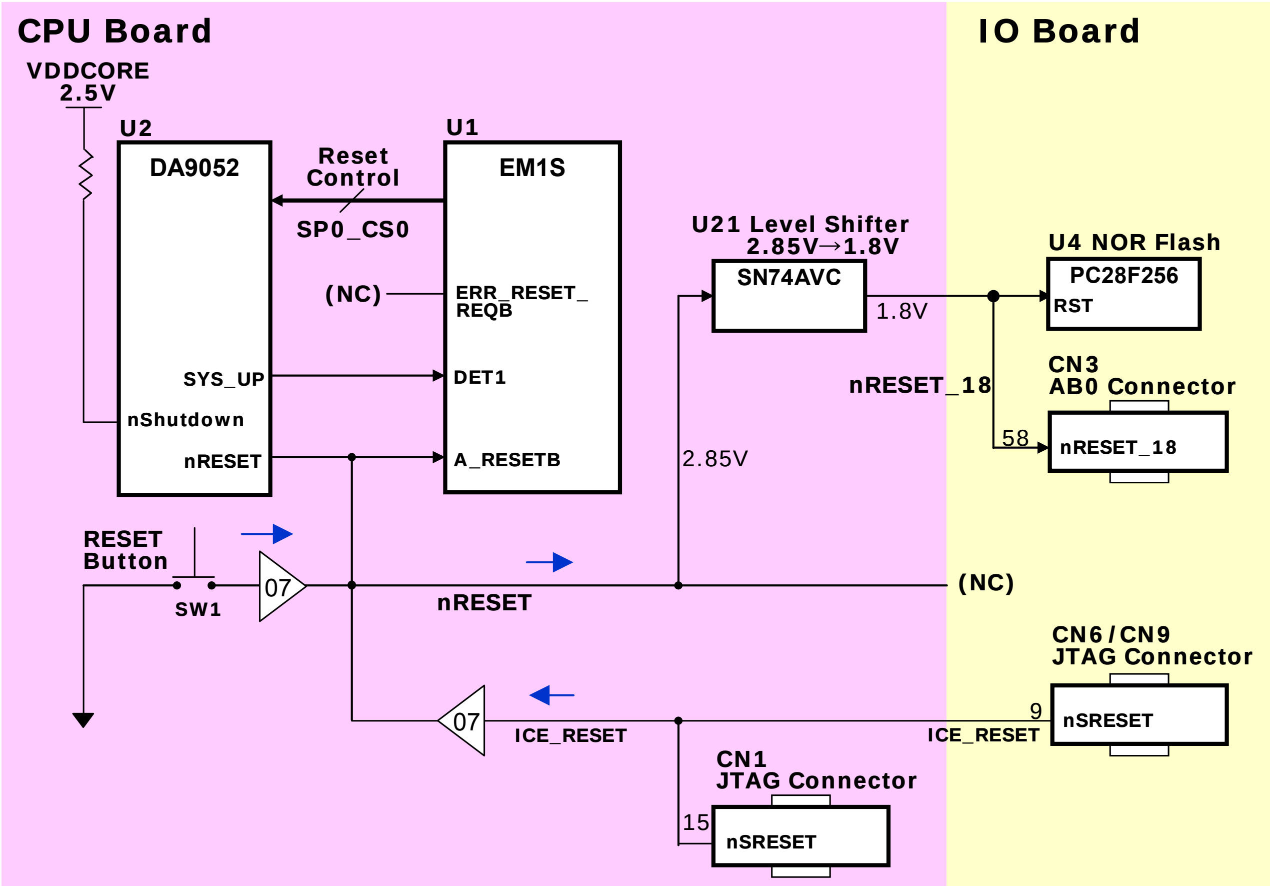


Figure 3-12 Reset System Architecture

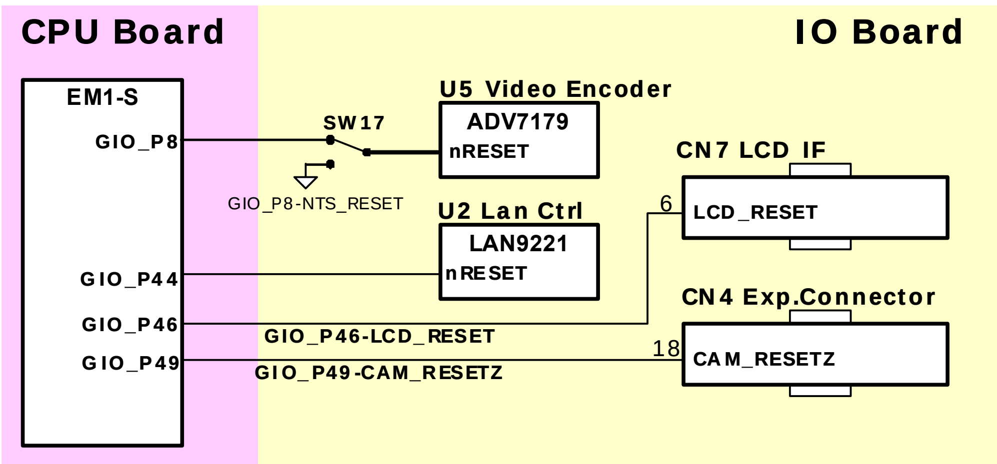


Figure 3-13 GPIO Base Reset System for IO Board

3.6. On Board Interrupts

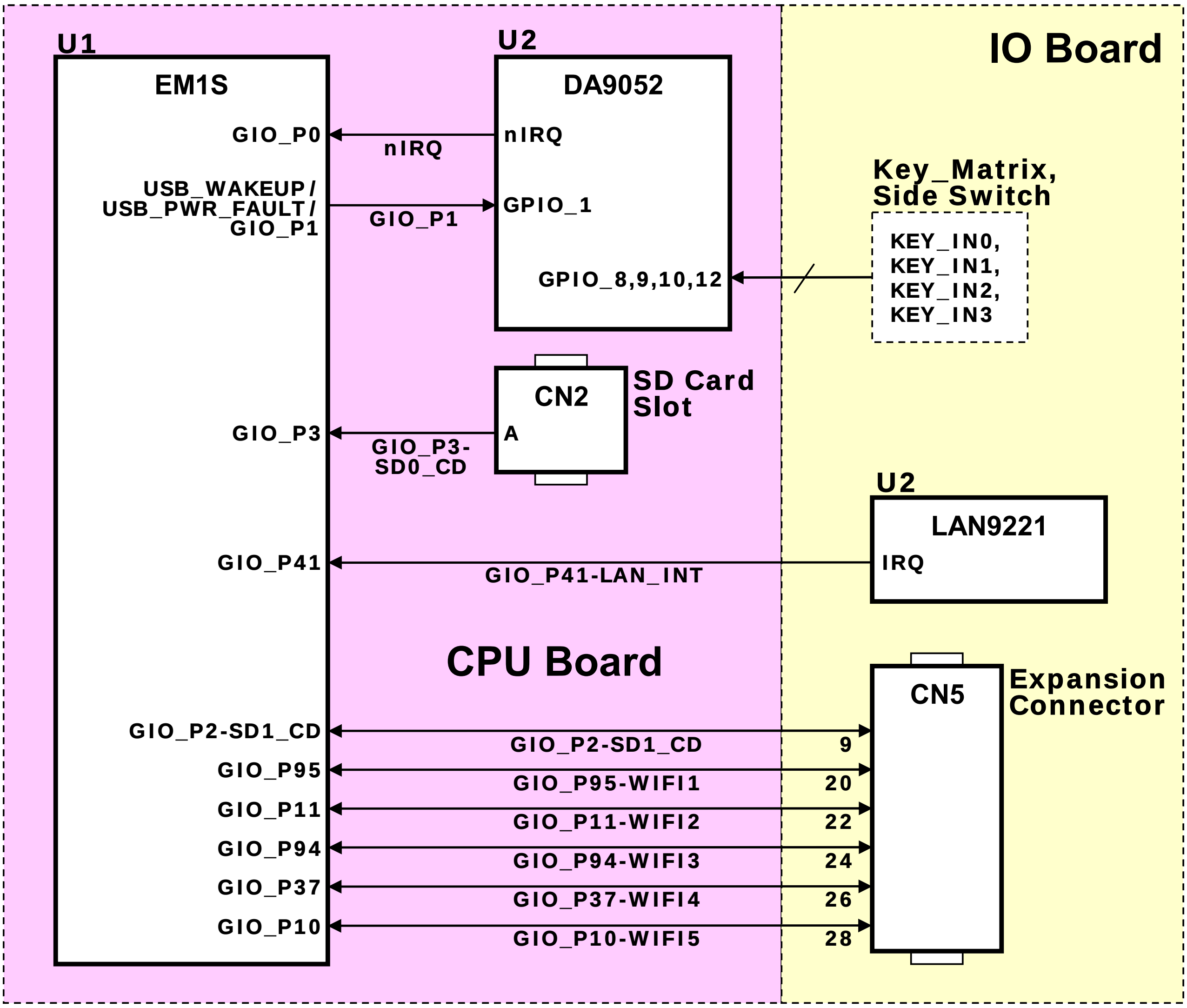


Figure 3-14 IRQ Tree of EM1 Development Kit Board

3.7. GPIO

EM1, DA9052, and MAX7324 have GPIO. Each GPIO is described blow.

3.7.1. EMMA Mobile1

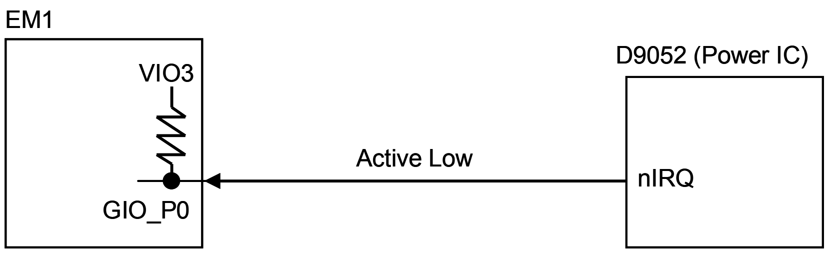
Table 3-4 EM1 GPIO Settings

<R>

GIO of EM1	Voltage[V] (Note 2)	I/O	Alternative function	Connected to	Board Revision (Note 1)
GIO_P0	VIO3	in	dedicated	D9052_nIRQ	
GIO_P2	VIO3	in	dedicated	Card Detect for SD1	
GIO_P3	VIO3	in	dedicated	Card Detect for SD0	
GIO_P4	VIO3	out	NAND_RB1	CAMSTANDBY	
GIO_P5	VIO3	out	NAND_RB2 CAM_SCLK	CAM_SCLK	
GIO_P6	VIO3	out	NAND_RB3	NAND /WP	
GIO_P8	VIO3	out	NAND_CE1	NTSC ADC7179 /RESET	
GIO_P9	VIO3	out	NAND_CE2	Audio AK4648 PDN	
GIO_P10	VIO3	in	NAND_CE3	WIFI5（SPI_INT to EM1）	
GIO_P11	VIO18	out	AB0_CLK	WIFI2（BT_Wakeup）	
GIO_P36	VIO18	in	AB0_A25	PushSW1	
GIO_P37	VIO18	out	AB0_A26	WIFI4（WL_Wakeup）	
GIO_P41	VIO18	in	AB0_WAIT	LAN 9221 IRQ	
GIO_P44	VIO18	out	AB0_CSB2	LAN9221 RESET	
GIO_P46	VIO18	out	AB0_BEN0	LCD_RESET	
GIO_P47	VIO18	out	AB0_BEN1	ISP1507 CS_N/PWRDN	Revision 1
				USB3329 RESETB	Revision 2
GIO_P49	VIO3	out	SP0_CS2	CAM_RESETZ	
GIO_P71	VIO18	in	LCD_ENABLE	PushSW2	
GIO_P94	VIO3	out	PWM0	WIFI3（WL_RESET）	
GIO_P95	VIO3	out	PWM1	WIFI1（BT_RESET）	

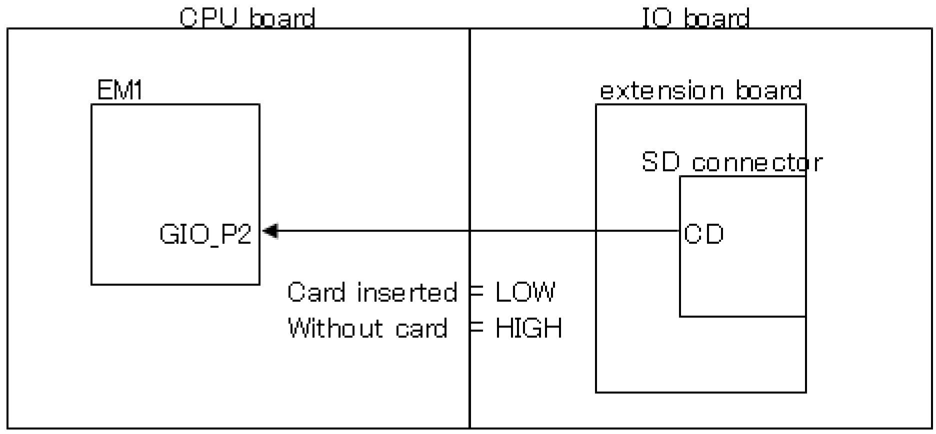
Note:
(1) Regarding Board revision, please refer to 5.5 Board Revision and 5.6 Board Information in EEPROM.
(2) VIO3 and VIO18 are depended on DA9052 programming. The concrete voltage can refer to 3.3.2 EM1-DA9052 Connection

GIO_P0

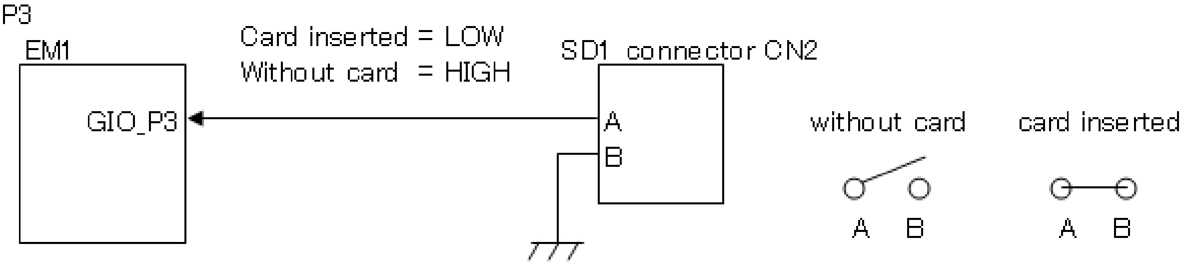


GIO_P0 is connected to DA9052 nIRQ which is open drain interface.
EM1 must receive the signal with an internal pull-up resistor and must set GIO_P0 as interrupt input.

GIO_P2

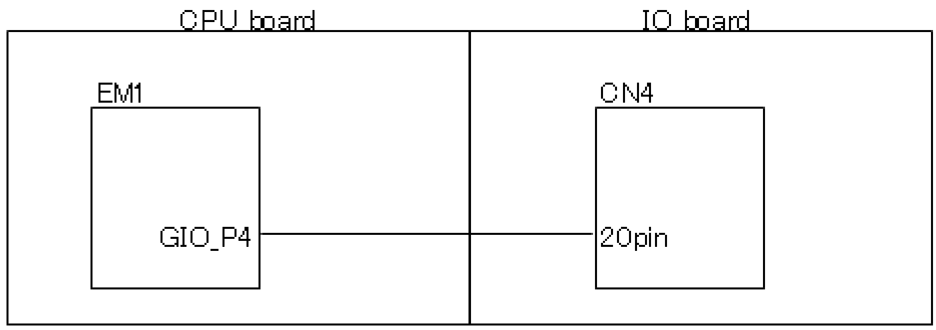


GIO_P3

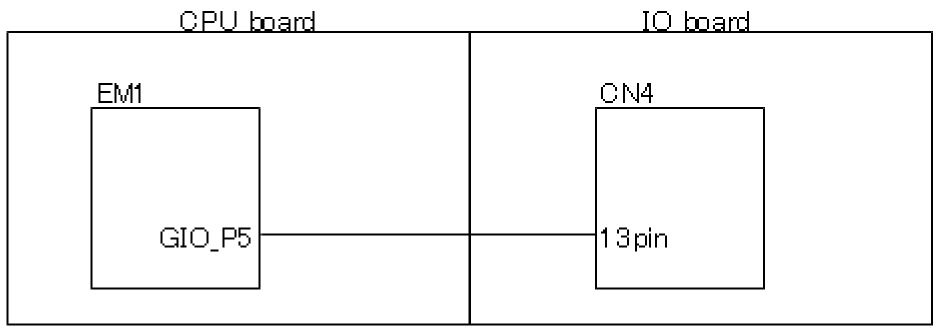


GIO_P3 must be set to pull up.

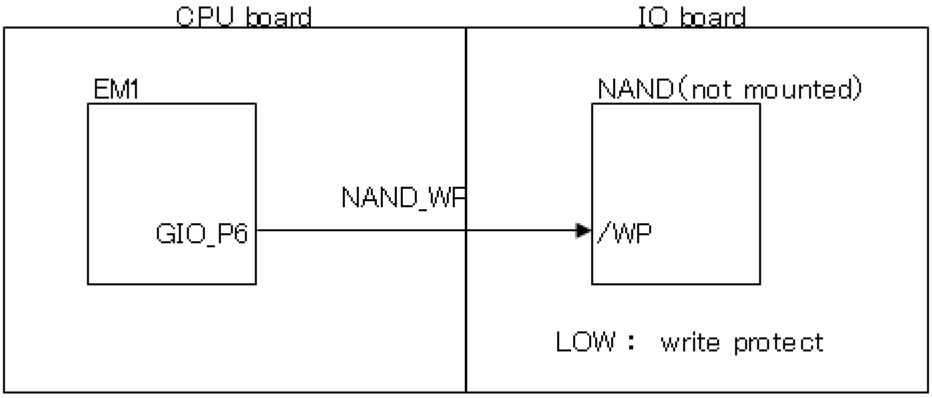
GIO_P4



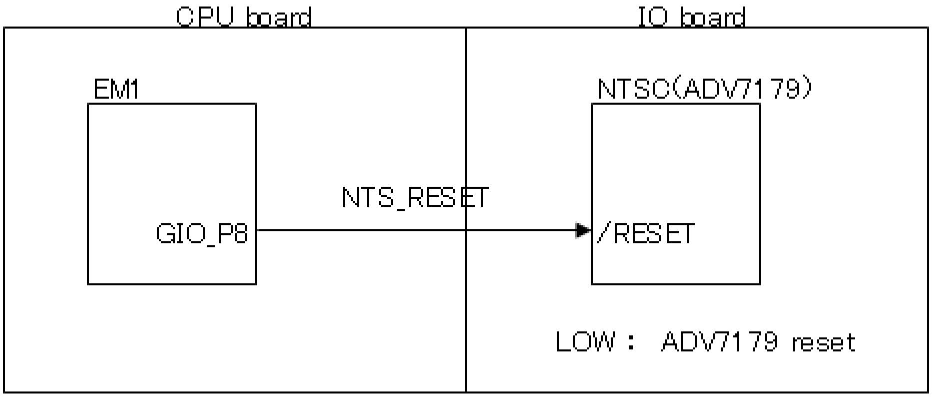
GIO_P5



GIO_P6



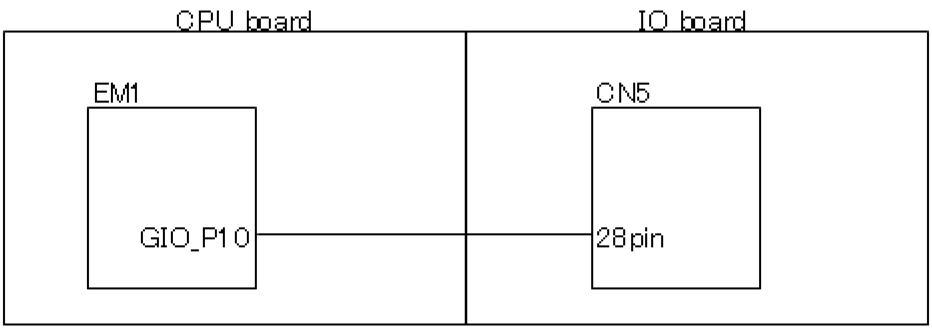
GIO_P8



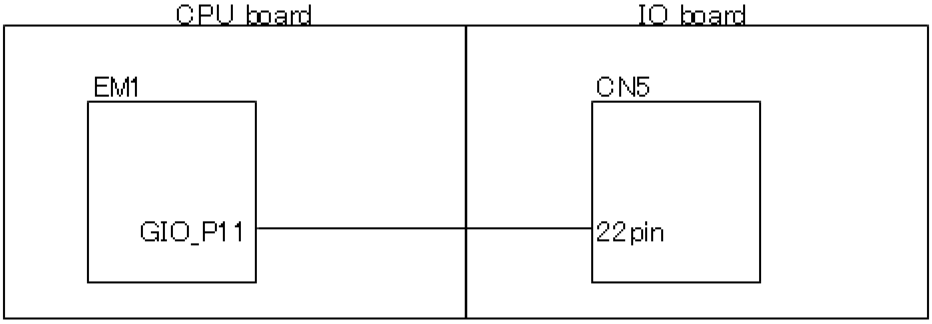
GIO_P9



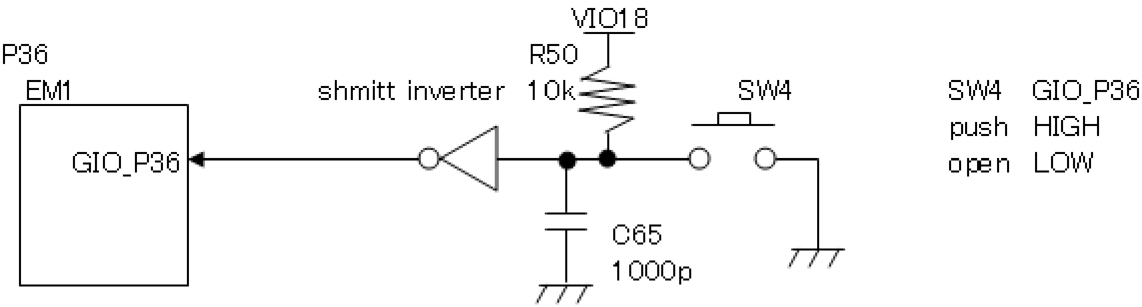
GIO_P10



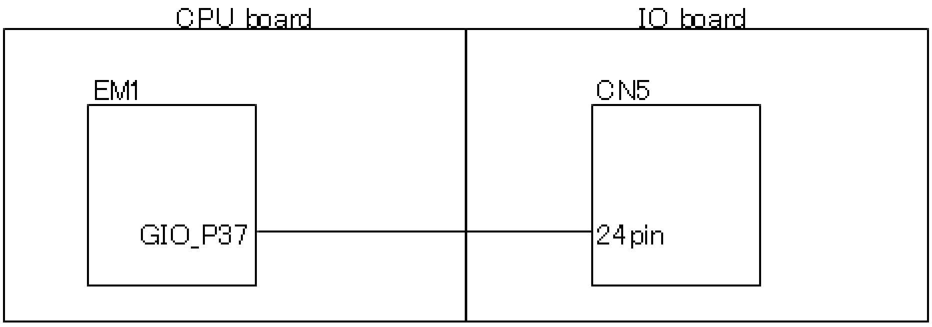
GIO_P11



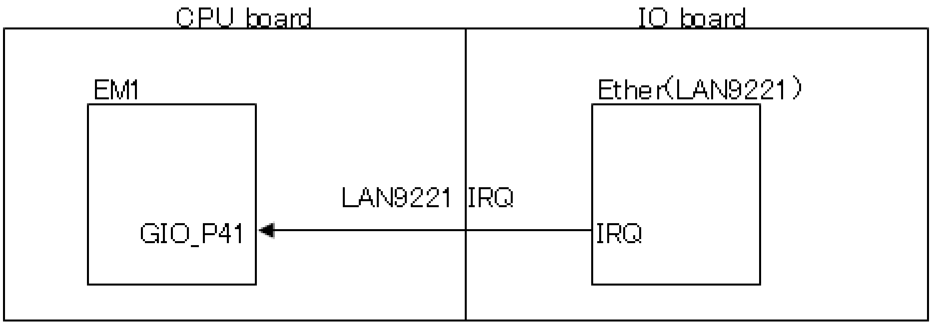
GIO_P36



GIO_P37

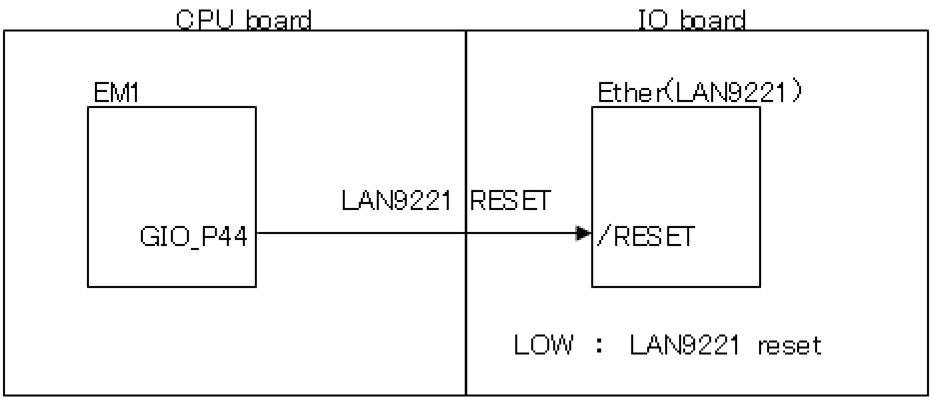


GIO_41

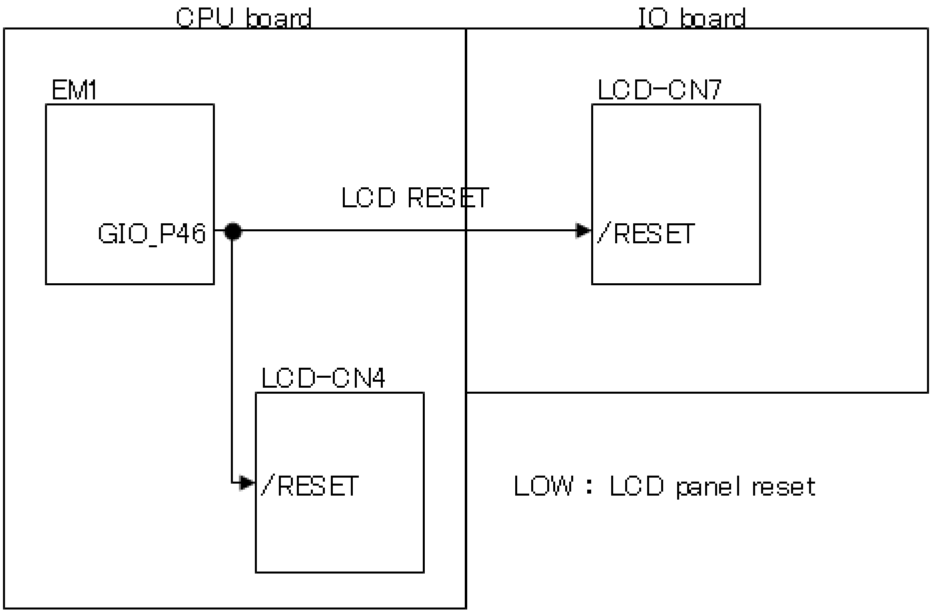


IRQ : active level programmable
To keep software compatibility with 91C111,
set IRQ active levet to HIGH.
IRQ_CFG regisiter bit4(IRQ Polarity) = 1 active HIGH
IRQ_CFG register bit0(IRQ buffer type) = 1 PushPull type

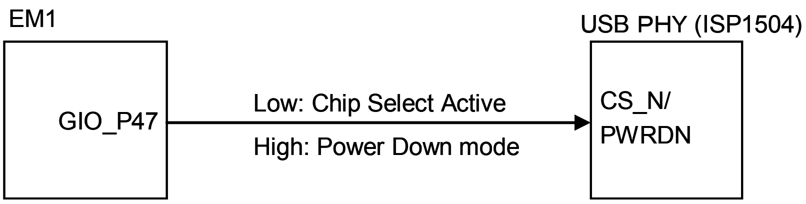
GIO_44



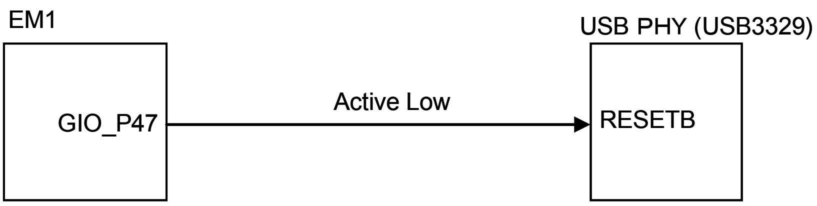
GIO_46



GIO_P47 for Board revision 1 (*)

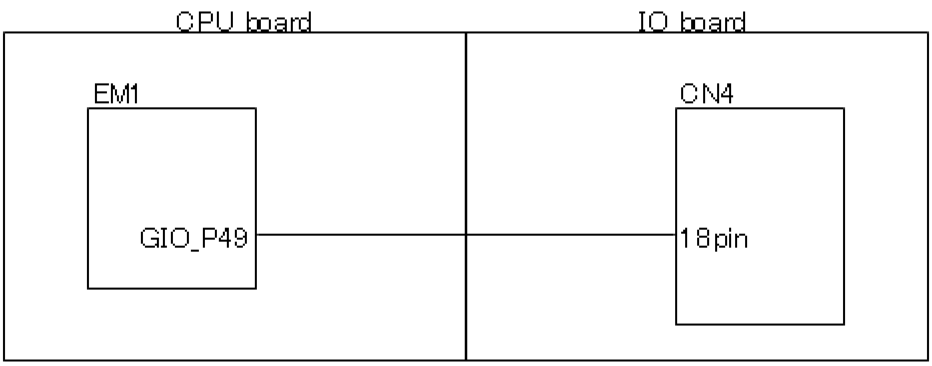


GIO_P47 for Board revision 2 (*)

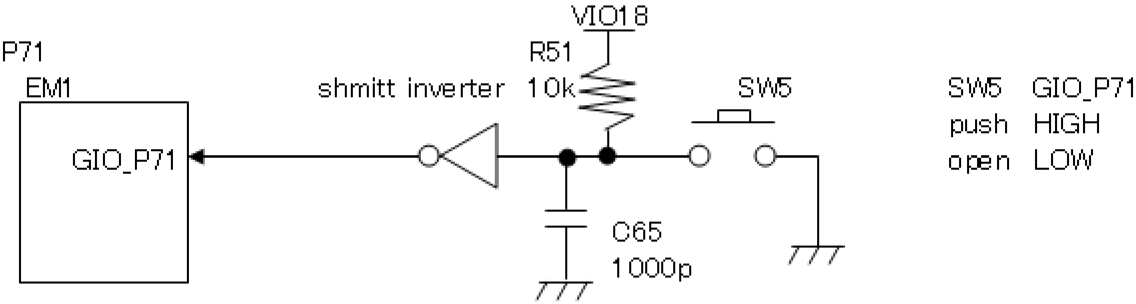


Note) Regarding Board revision, please refer to 5.5 Board Revision and 5.6 Board Information in EEPROM.

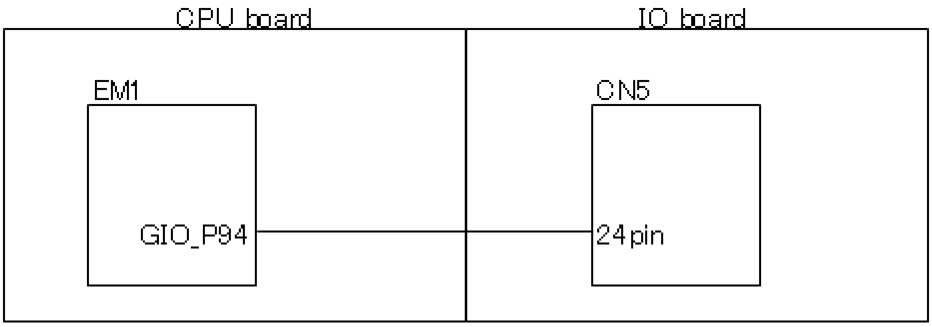
GIO_P49



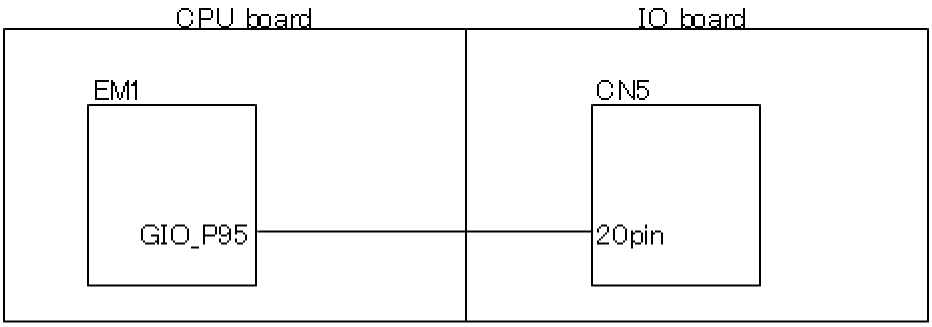
GIO_P71



GIO_P94



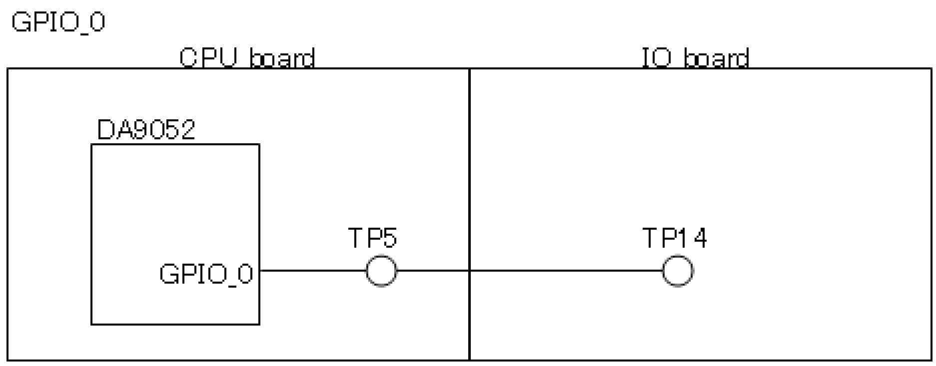
GIO_P95



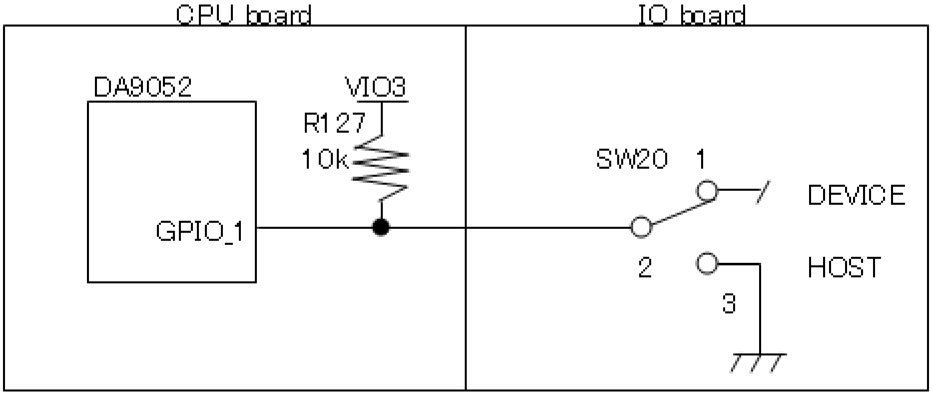
3.7.2. DA9052

Table 3-5 DA9052 GPIO

DA9052	I/O	Alternative function	Selected function	Connected to	Board revision
GPIO_0	out	ADCIN4		PAD	
GPIO_1	in	ADCIN5		USB-mode DIPSW	
GPIO_2	in	ADCIN6		USB_WAKEUP	
GPIO_3	in	TSIYN	TSIYN	LCD CN4-44 YD	
GPIO_4	in	TSIYP	TSIYP	LCD CN4-46 YU	
GPIO_5	in	TSIXN	TSIXN	LCD CN4-43 XL	
GPIO_6	in	TSIXP	TSIXP	LCD CN4-45 XR	
GPIO_7	in	TSREF	TSREF	DA9052 VLDO9	
GPIO_8	in	SYS_EN		key_in0	
GPIO_9	in	PWR_EN		key_in1	
GPIO_10	in	PWR1_EN		key_in2	
GPIO_11	in	ACC_ID_DET	ACC_ID_DET	USB ID for CN5	
GPIO_12	in	GP_FB1		key_in3	
GPIO_13	out	nVDD_FAULT	nVDD_FAULT	CN9-1pin	Revision 1
				MAX1946 ON/OFF	Revision 2
GPIO_14	out	DATA		LED1	
GPIO_15	out	CLK		LED2	



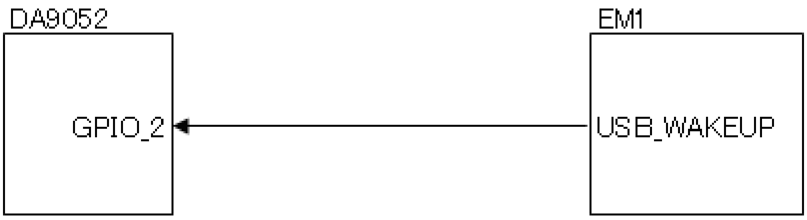
GPIO_1



USB HOST/DEVICE mode change switch definition

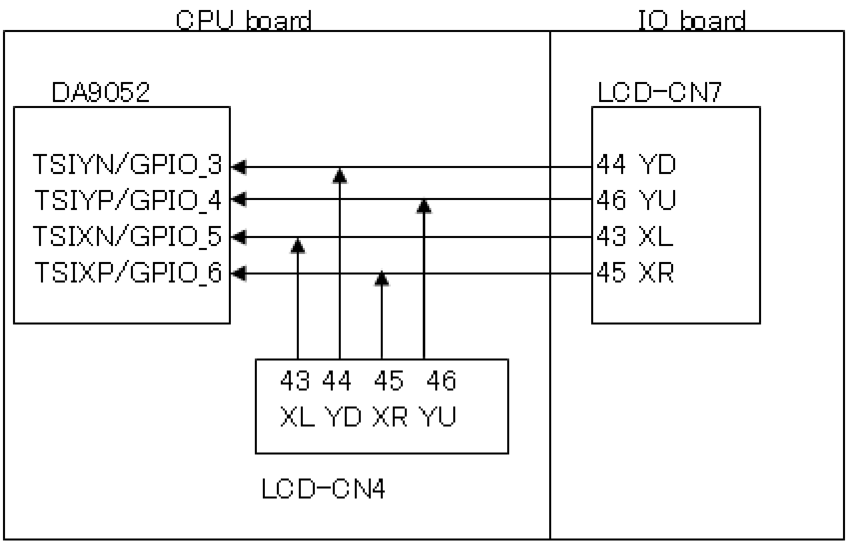
	SW20	GPIO_1
DEVICE	1-2	HIGH
HOST	2-3	LOW

GPIO_2

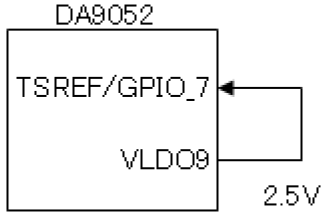


GPIO_2 is connected to USB_WAKEUP signal as an interrupt factor.

TSIYX,TSIYP,TSIXN,TSIXP(GPIO_3,4,5,6)

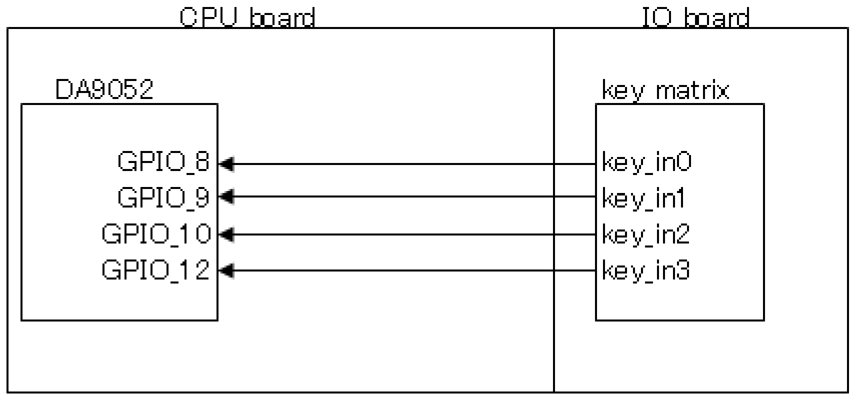


TSREF(GPIO_7)

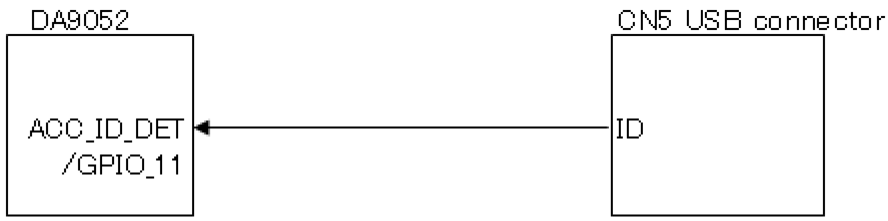


TSREF is connected to VLDO9(2.5V). It is a reference voltage of touch panel interface.

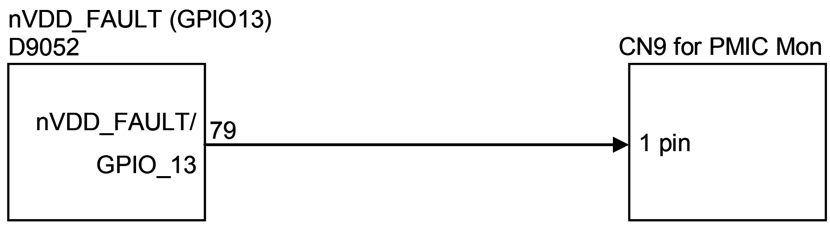
GPIO_8, GPIO_9, GPIO_10, GPIO_12



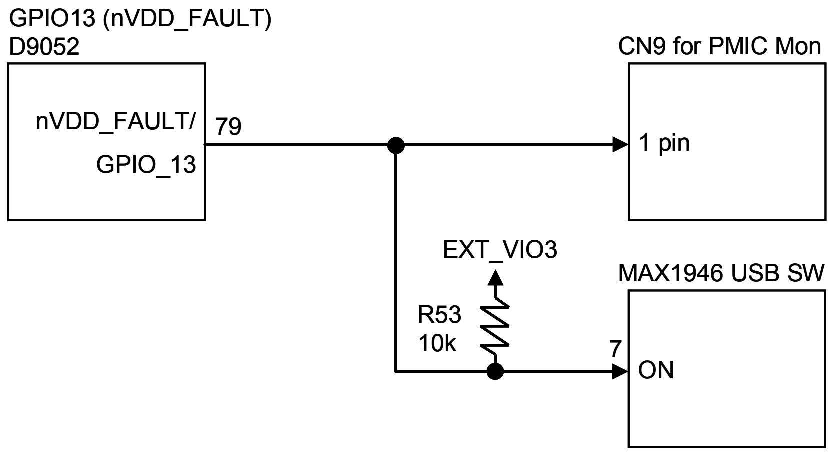
ACC_ID_DET(GPIO_11)



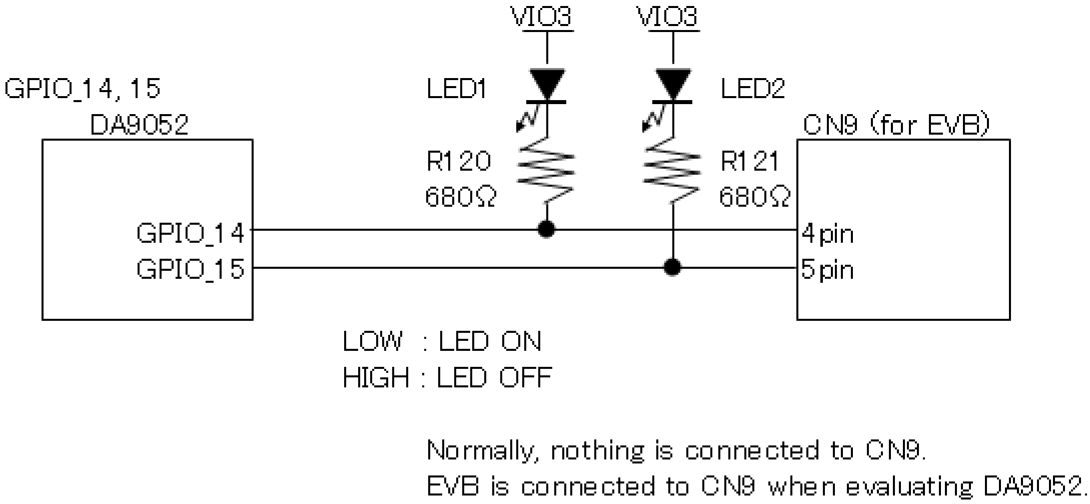
GPIO13 for Board Revision 1 (*)



GPIO13 for Board Revision 2 (*)



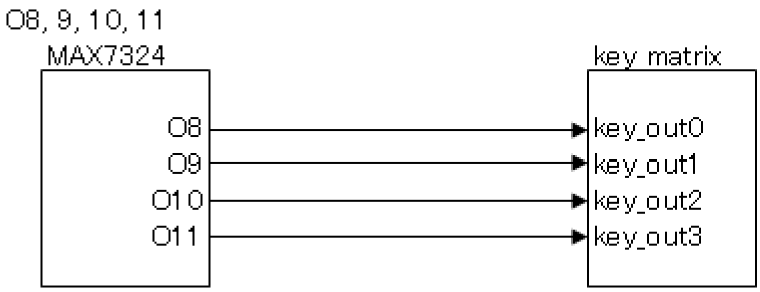
Note) Regarding Board revision, please refer to 5.5 Board Revision and 5.6 Board Information in EEPROM.

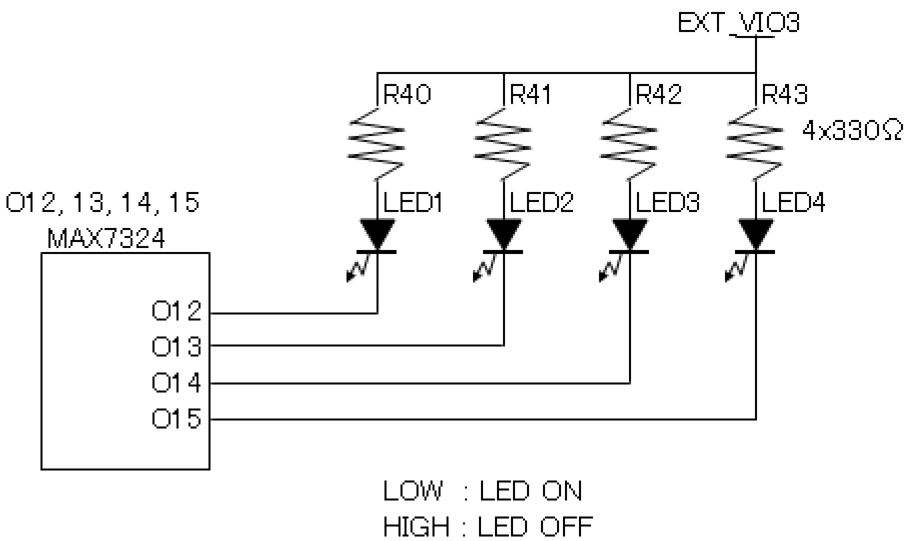


3.7.3. MAX7324

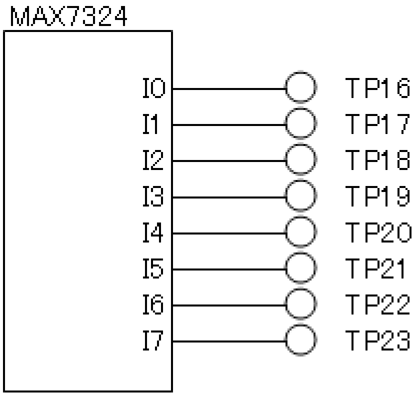
Table 3-6 MAX7324 GPIO

MAX7324 GPIO	I/O	connect to	initial condition
O8	out	key matrix key_out0	High
O9	out	key matrix key_out1	High
O10	out	key matrix key_out2	High
O11	out	key matrix key_out3	High
O12	out	LED1	High
O13	out	LED2	High
O14	out	LED3	High
O15	out	LED4	High
I0	in	TP16	internal 40k pull-up anytime
I1	in	TP17	internal 40k pull-up anytime
I2	in	TP18	internal 40k pull-up anytime
I3	in	TP19	internal 40k pull-up anytime
I4	in	TP20	internal 40k pull-up anytime
I5	in	TP21	internal 40k pull-up anytime
I6	in	TP22	internal 40k pull-up anytime
I7	in	TP23	internal 40k pull-up anytime



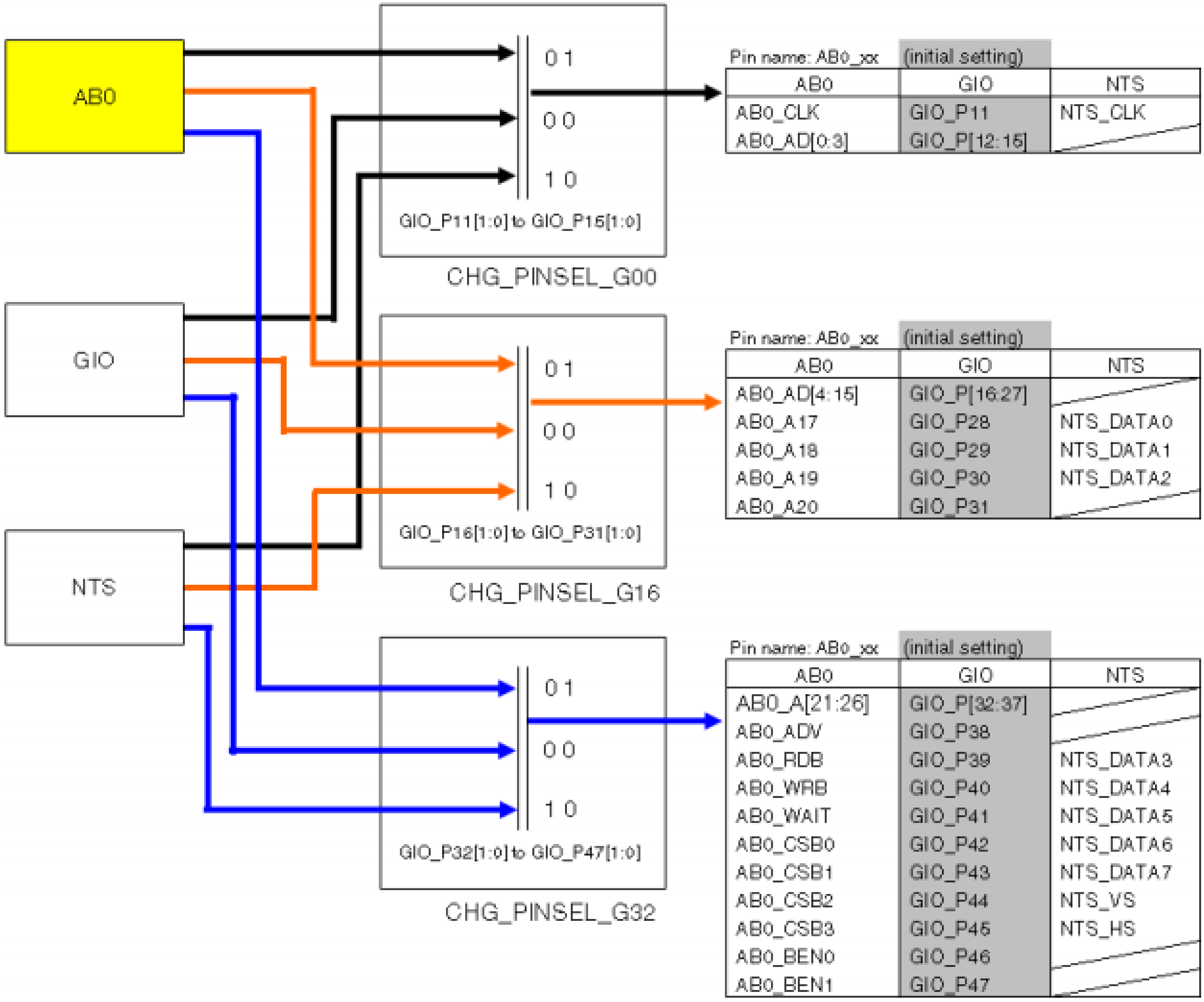


I0, I1 , I2, I3, I4, I5, I6, I7



3.8. Pin setting

3.8.1. AB0



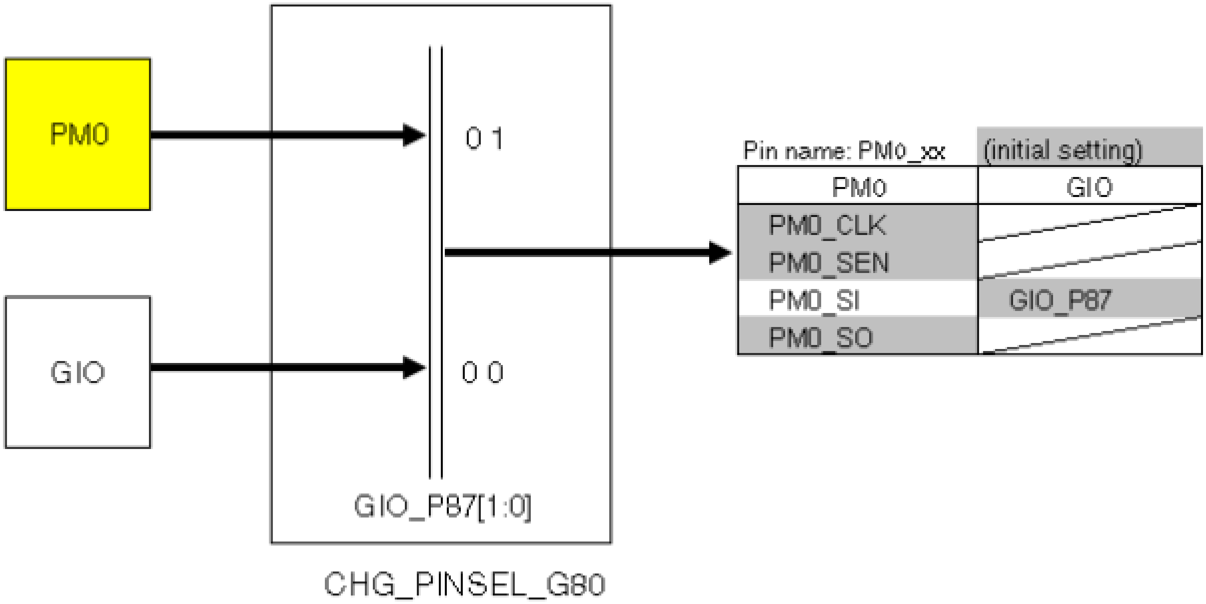
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G00 C014_0200H	[31:30]	GIO_P15	AB0_AD3			01b
	[29:28]	GIO_P14	AB0_AD2			01b
	[27:26]	GIO_P13	AB0_AD1			01b
	[25:24]	GIO_P12	AB0_AD0			01b
	[23:22]	GIO_P11	AB0_CLK	NTS_CLK		00b
	[21:20]	GIO_P10		NAND_CE3		00b
	[19:18]	GIO_P9		NAND_CE2		00b
	[17:16]	GIO_P8		NAND_CE1		00b
	[15:14]	GIO_P7		NAND_CE0		10b
	[13:12]	GIO_P6		NAND_RB3		00b
	[11:10]	GIO_P5		NAND_RB2		00b
	[9:8]	GIO_P4		NAND_RB1		00b
	[7:6]	GIO_P3				00b
	[5:4]	GIO_P2				00b
	[3:2]	GIO_P1	USB_WAKEUP	USB_PWR_FAULT		01b
	[1:0]	GIO_P0				00b

		alternative pins	

Register	bit	00b	01b	10b	set value
CHG_PINSEL_G16 C014_0204H	[31:30]	GIO_P31	AB0_A20		01b
	[29:28]	GIO_P30	AB0_A19	NTS_DATA2	01b
	[27:26]	GIO_P29	AB0_A18	NTS_DATA1	01b
	[25:24]	GIO_P28	AB0_A17	NTS_DATA0	01b
	[23:22]	GIO_P27	AB0_AD15		01b
	[21:20]	GIO_P26	AB0_AD14		01b
	[19:18]	GIO_P25	AB0_AD13		01b
	[17:16]	GIO_P24	AB0_AD12		01b
	[15:14]	GIO_P23	AB0_AD11		01b
	[13:12]	GIO_P22	AB0_AD10		01b
	[11:10]	GIO_P21	AB0_AD9		01b
	[9:8]	GIO_P20	AB0_AD8		01b
	[7:6]	GIO_P19	AB0_AD7		01b
	[5:4]	GIO_P18	AB0_AD6		01b
	[3:2]	GIO_P17	AB0_AD5		01b
	[1:0]	GIO_P16	AB0_AD4		01b

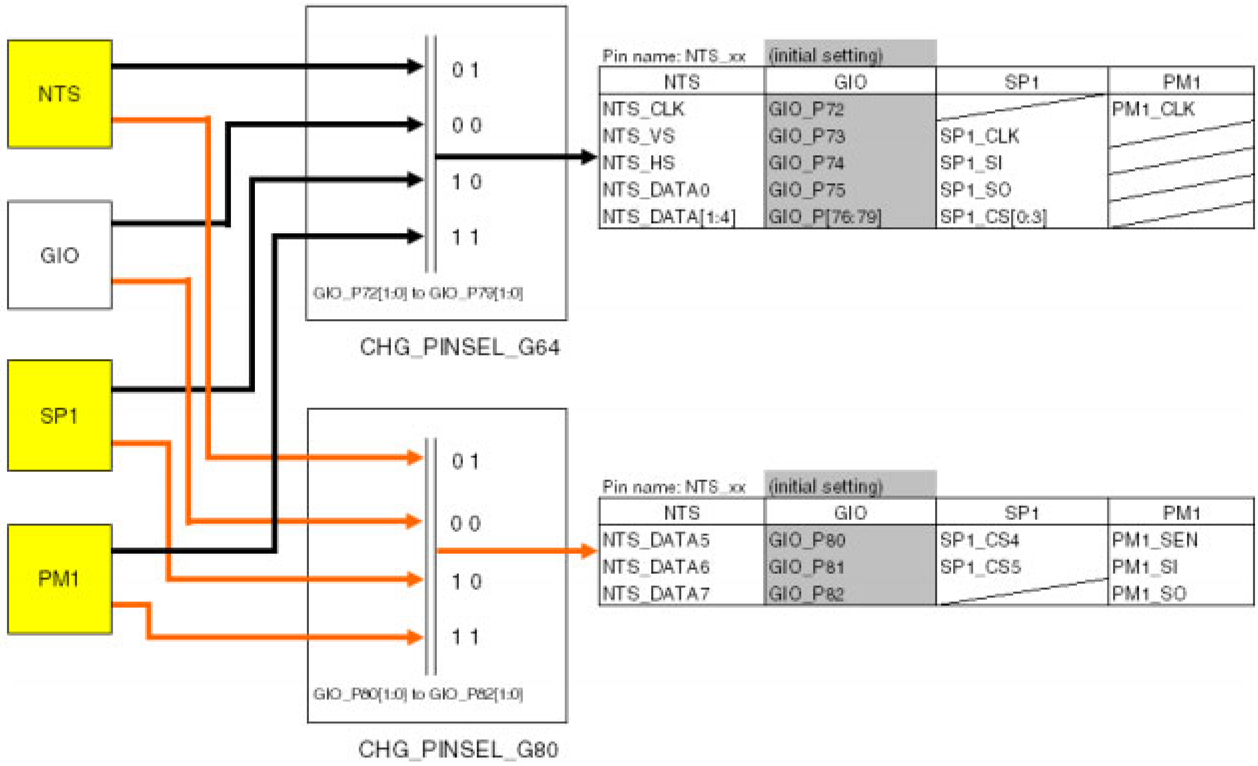
		alternative pins list			
Register	bit	00b	01b	10b	set value
CHG_PINSEL_G32 C014_0208	[31:30]	GIO_P47	AB0_BEN1		00b
	[29:28]	GIO_P46	AB0_BEN0		00b
	[27:26]	GIO_P45	AB0_CSB3	NTS_HS	00b
	[25:24]	GIO_P44	AB0_CSB2	NTS_VS	00b
	[23:22]	GIO_P43	AB0_CSB1	NTS_DATA7	00b
	[21:20]	GIO_P42	AB0_CSB0	NTS_DATA6	01b
	[19:18]	GIO_P41	AB0_WAIT	NTS_DATA5	00b
	[17:16]	GIO_P40	AB0_WRB	NTS_DATA4	01b
	[15:14]	GIO_P39	AB0_RDB	NTS_DATA3	01b
	[13:12]	GIO_P38	AB0_ADV		01b
	[11:10]	GIO_P37	AB0_A26		00b
	[9:8]	GIO_P36	AB0_A25		00b
	[7:6]	GIO_P35	AB0_A24		01b
	[5:4]	GIO_P34	AB0_A23		01b
	[3:2]	GIO_P33	AB0_A22		01b
	[1:0]	GIO_P32	AB0_A21		01b

3.8.2. PM0



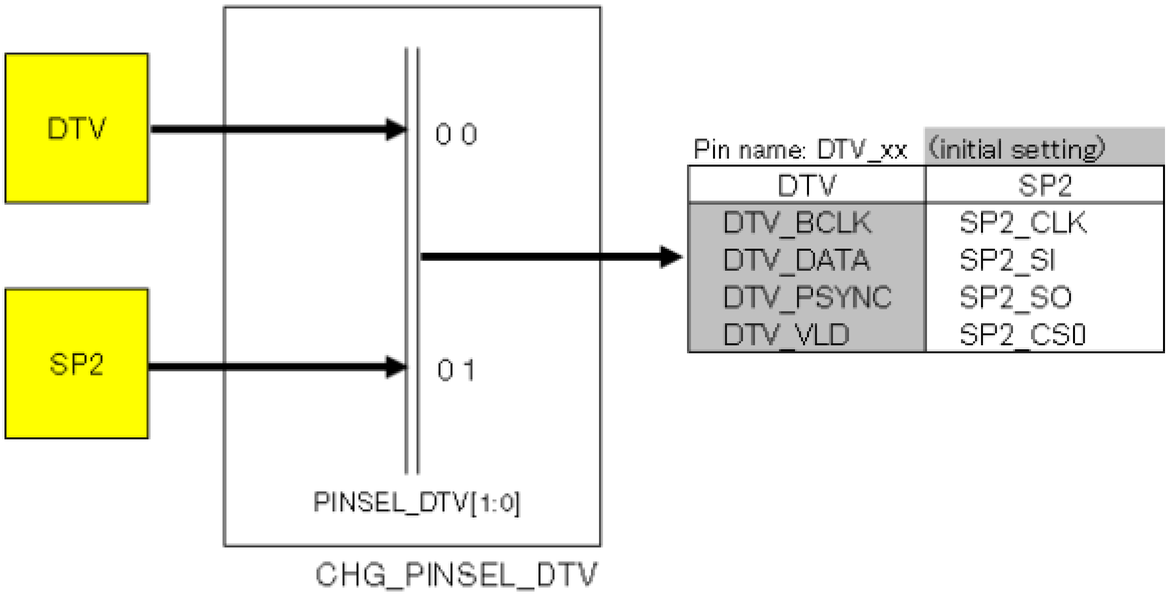
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G80 C014_0214	[31:30]	GIO_P95	PWM1			00b
	[29:28]	GIO_P94	PWM0			00b
	[27:26]	GIO_P93	SD2_CKI	NAND_OE		01b
	[25:24]	GIO_P92	SD1_CKI	CAM_CLKI		01b
	[23:22]	GIO_P91	SD0_CKI			01b
	[21:20]	GIO_P90	SD0_DATA3			01b
	[19:18]	GIO_P89	SD0_DATA2			01b
	[17:16]	GIO_P88	SD0_DATA1			01b
	[15:14]	GIO_P87	PM0_SI			01b
	[13:12]	GIO_P86	URT0_RTSB	URT1_SOUT		10b
	[11:10]	GIO_P85	URT0_CTSB	URT1_SRIN		10b
	[9:8]	GIO_P84	IIC_SDA			01b
	[7:6]	GIO_P83	IIC_SCL			01b
	[5:4]	GIO_P82	NTS_DATA7	PM1_SO	PM1_SO	01b
	[3:2]	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	01b
	[1:0]	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	01b

3.8.3. NTS,SP1



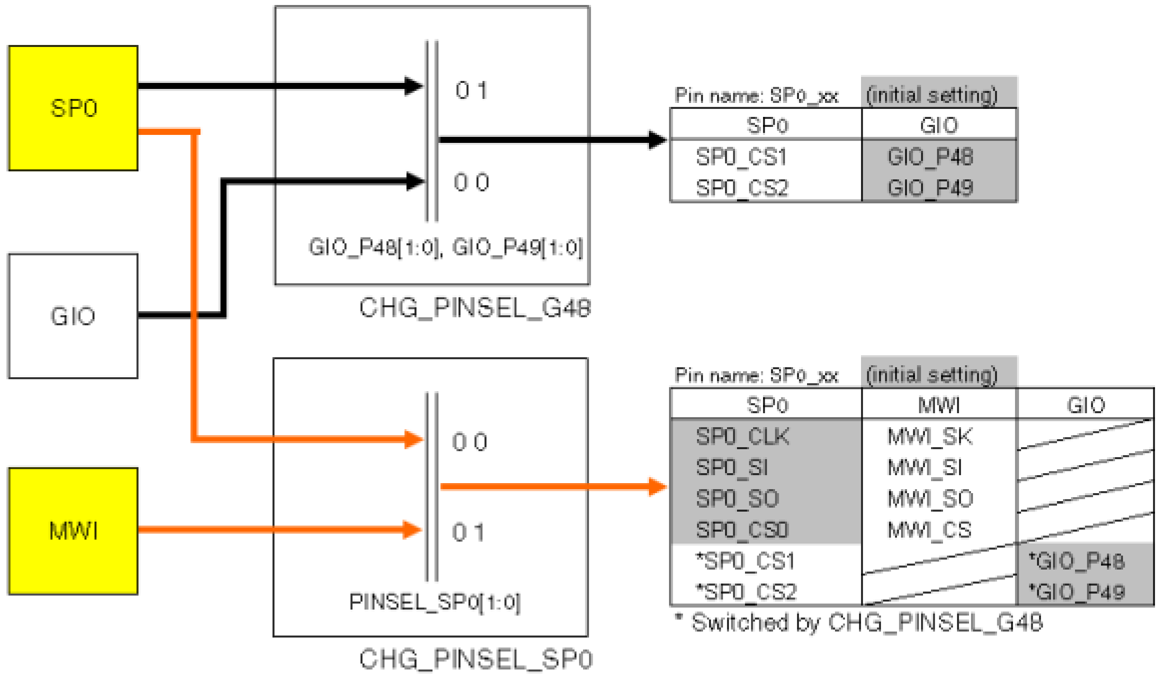
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G64 C014_0210	[31:30]	GIO_P79	NTS_DATA4	SP1_CS3	CAM_YUV4	01b
	[29:28]	GIO_P78	NTS_DATA3	SP1_CS2	CAM_YUV3	01b
	[27:26]	GIO_P77	NTS_DATA2	SP1_CS1	CAM_YUV2	01b
	[25:24]	GIO_P76	NTS_DATA1	SP1_CS0	CAM_YUV1	01b
	[23:22]	GIO_P75	NTS_DATA0	SP1_SO	CAM_YUV0	01b
	[21:20]	GIO_P74	NTS_HS	SP1_SI		01b
	[19:18]	GIO_P73	NTS_VS	SP1_CLK		01b
	[17:16]	GIO_P72	NTS_CLK		PM1_CLK	01b
	[15:14]	GIO_P71	LCD_ENABLE			01b
	[13:12]	GIO_P70	LCD_VSYNC			01b
	[11:10]	GIO_P69	LCD_HSYNC			01b
	[9:8]	GIO_P68	LCD_B5			01b
	[7:6]	GIO_P67	LCD_B4			01b
	[5:4]	GIO_P66	LCD_B3			01b
	[3:2]	GIO_P65	LCD_B2			01b
	[1:0]	GIO_P64	LCD_B1			01b

3.8.4. DTV,SP2



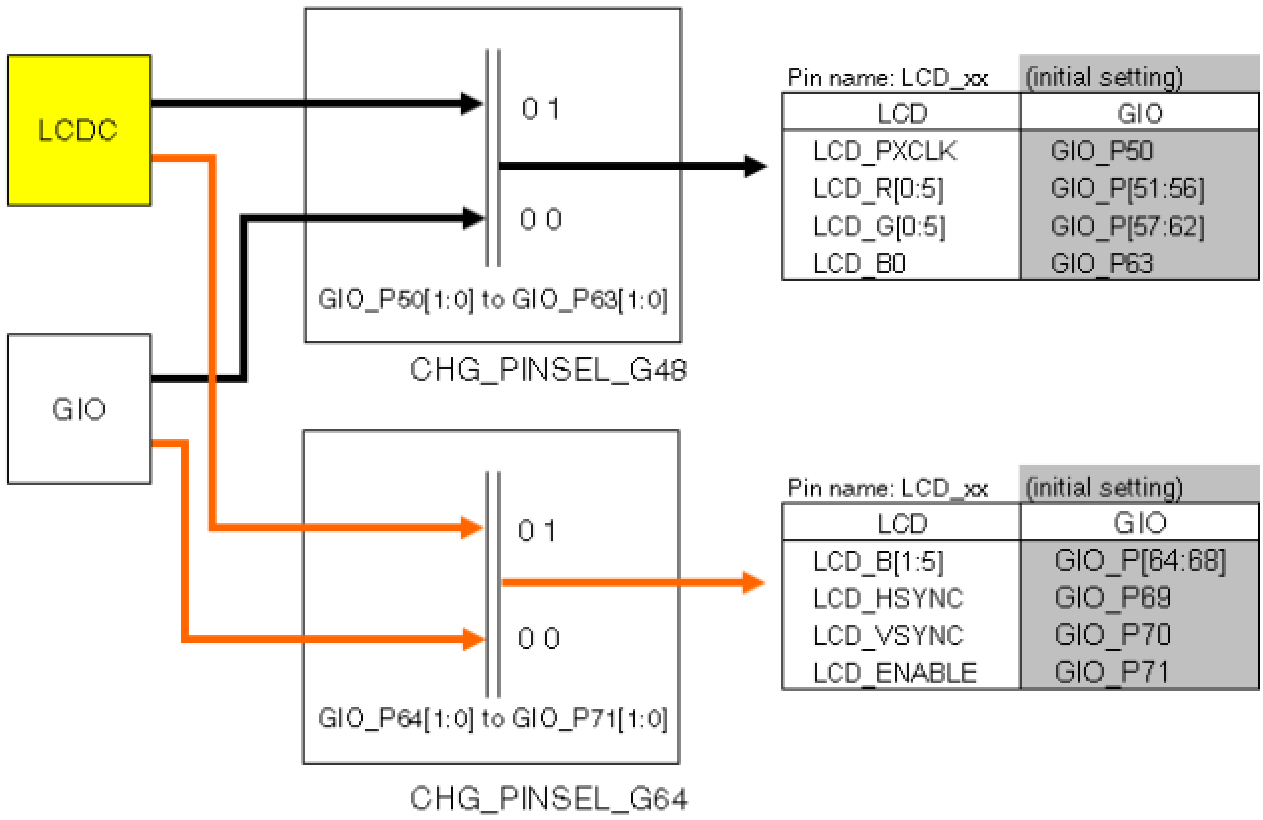
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_DTV C014_0284	[31:30]					
	[29:28]					
	[27:26]					
	[25:24]					
	[23:22]					
	[21:20]					
	[19:18]					
	[17:16]					
	[15:14]					
	[13:12]					
	[11:10]					
	[9:8]					
	[7:6]					
	[5:4]					
	[3:2]					
	[1:0]	DTV	SP2			00b

3.8.5. SP0,MMI



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_SP0 C014_0280	[31:30]					
	[29:28]					
	[27:26]					
	[25:24]					
	[23:22]					
	[21:20]					
	[19:18]					
	[17:16]					
	[15:14]					
	[13:12]					
	[11:10]					
	[9:8]					
	[7:6]					
	[5:4]					
	[3:2]					
	[1:0]	SP0, GIO	MWI, CS			00b

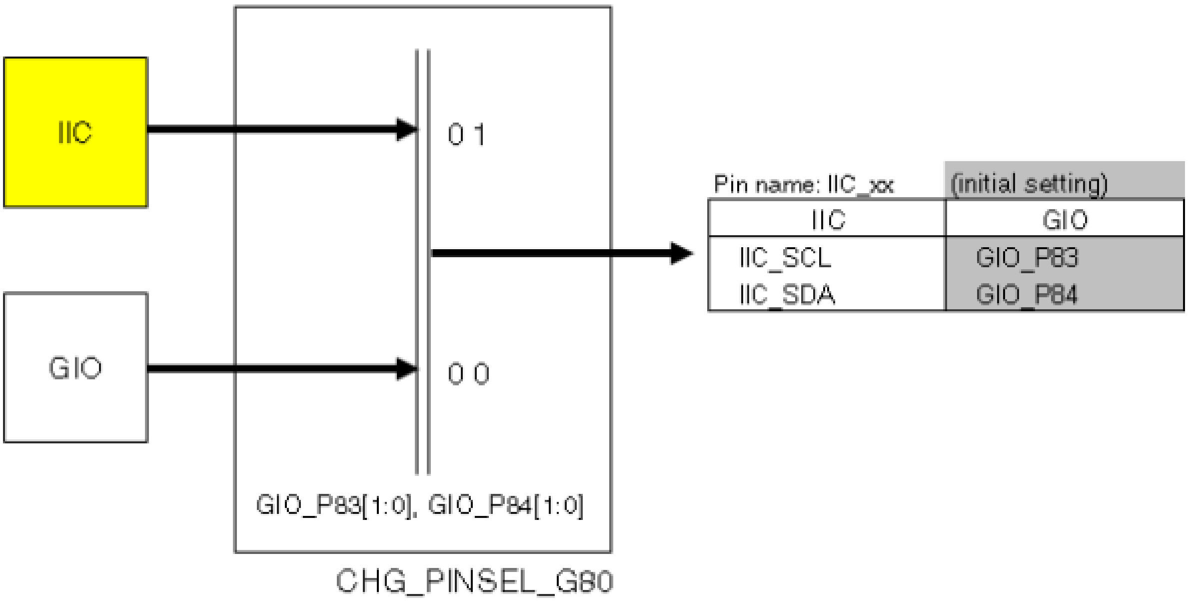
3.8.6. LCDC



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G48 C014_020C	[31:30]	GIO_P63	LCD_B0			01b
	[29:28]	GIO_P62	LCD_G5			01b
	[27:26]	GIO_P61	LCD_G4			01b
	[25:24]	GIO_P60	LCD_G3			01b
	[23:22]	GIO_P59	LCD_G2			01b
	[21:20]	GIO_P58	LCD_G1			01b
	[19:18]	GIO_P57	LCD_G0			01b
	[17:16]	GIO_P56	LCD_R5			01b
	[15:14]	GIO_P55	LCD_R4			01b
	[13:12]	GIO_P54	LCD_R3			01b
	[11:10]	GIO_P53	LCD_R2			01b
	[9:8]	GIO_P52	LCD_R1			01b
	[7:6]	GIO_P51	LCD_R0			01b
	[5:4]	GIO_P50	LCD_PXCLK			01b
	[3:2]	GIO_P49	SP0_CS2			00b
	[1:0]	GIO_P48	SP0_CS1			01b

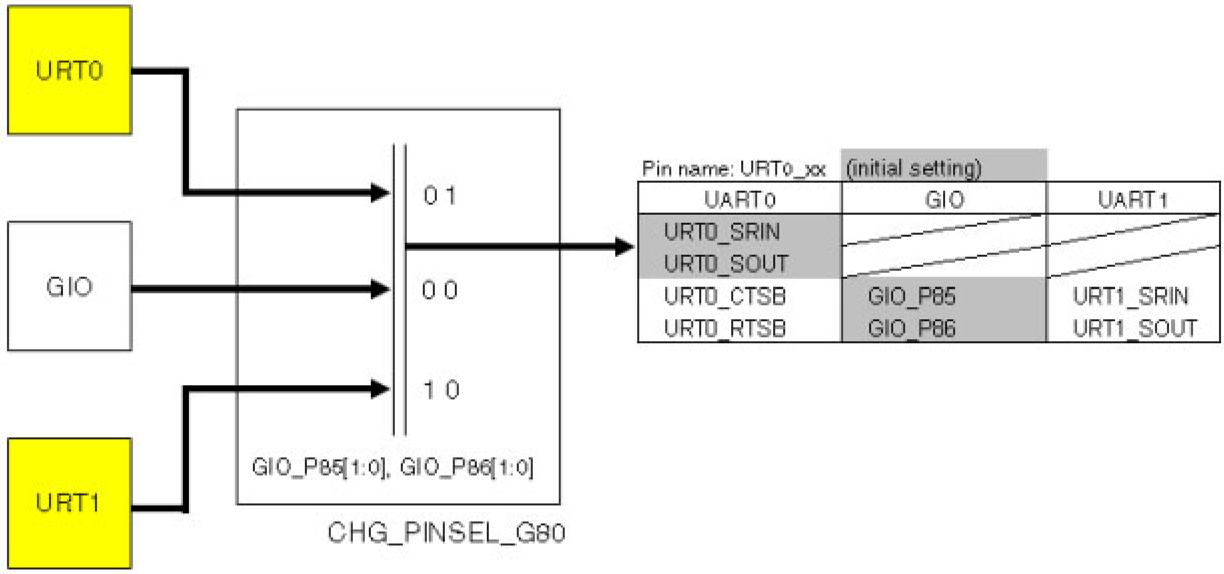
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G64 C014_0210	[31:30]	GIO_P79	NTS_DATA4	SP1_CS3	CAM_YUV4	01b
	[29:28]	GIO_P78	NTS_DATA3	SP1_CS2	CAM_YUV3	01b
	[27:26]	GIO_P77	NTS_DATA2	SP1_CS1	CAM_YUV2	01b
	[25:24]	GIO_P76	NTS_DATA1	SP1_CS0	CAM_YUV1	01b
	[23:22]	GIO_P75	NTS_DATA0	SP1_SO	CAM_YUV0	01b
	[21:20]	GIO_P74	NTS_HS	SP1_SI		01b
	[19:18]	GIO_P73	NTS_VS	SP1_CLK		01b
	[17:16]	GIO_P72	NTS_CLK		PM1_CLK	01b
	[15:14]	GIO_P71	LCD_ENABLE			01b
	[13:12]	GIO_P70	LCD_VSYNC			01b
	[11:10]	GIO_P69	LCD_HSYNC			01b
	[9:8]	GIO_P68	LCD_B5			01b
	[7:6]	GIO_P67	LCD_B4			01b
	[5:4]	GIO_P66	LCD_B3			01b
	[3:2]	GIO_P65	LCD_B2			01b
	[1:0]	GIO_P64	LCD_B1			01b

3.8.7. IIC



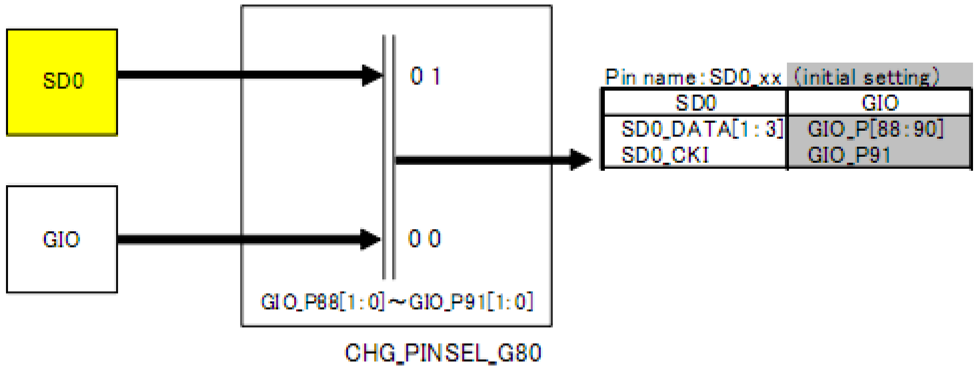
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G80 C014_0214	[31:30]	GIO_P95	PWM1			00b
	[29:28]	GIO_P94	PWM0			00b
	[27:26]	GIO_P93	SD2_CKI	NAND_OE		01b
	[25:24]	GIO_P92	SD1_CKI	CAM_CLKI		01b
	[23:22]	GIO_P91	SD0_CKI			01b
	[21:20]	GIO_P90	SD0_DATA3			01b
	[19:18]	GIO_P89	SD0_DATA2			01b
	[17:16]	GIO_P88	SD0_DATA1			01b
	[15:14]	GIO_P87	PM0_SI			01b
	[13:12]	GIO_P86	URT0_RTSB	URT1_SOUT		10b
	[11:10]	GIO_P85	URT0_CTSB	URT1_SRIN		10b
	[9:8]	GIO_P84	IIC_SDA			01b
	[7:6]	GIO_P83	IIC_SCL			01b
	[5:4]	GIO_P82	NTS_DATA7	PM1_SO	PM1_SO	01b
	[3:2]	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	01b
	[1:0]	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	01b

3.8.8. URT0, URT1



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G80 C014_0214	[31:30]	GIO_P95	PWM1			00b
	[29:28]	GIO_P94	PWM0			00b
	[27:26]	GIO_P93	SD2_CKI	NAND_OE		01b
	[25:24]	GIO_P92	SD1_CKI	CAM_CLKI		01b
	[23:22]	GIO_P91	SD0_CKI			01b
	[21:20]	GIO_P90	SD0_DATA3			01b
	[19:18]	GIO_P89	SD0_DATA2			01b
	[17:16]	GIO_P88	SD0_DATA1			01b
	[15:14]	GIO_P87	PM0_SI			01b
	[13:12]	GIO_P86	URT0_RTSB	URT1_SOUT		10b
	[11:10]	GIO_P85	URT0_CTSB	URT1_SRIN		10b
	[9:8]	GIO_P84	IIC_SDA			01b
	[7:6]	GIO_P83	IIC_SCL			01b
	[5:4]	GIO_P82	NTS_DATA7	PM1_SO	PM1_SO	01b
	[3:2]	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	01b
	[1:0]	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	01b

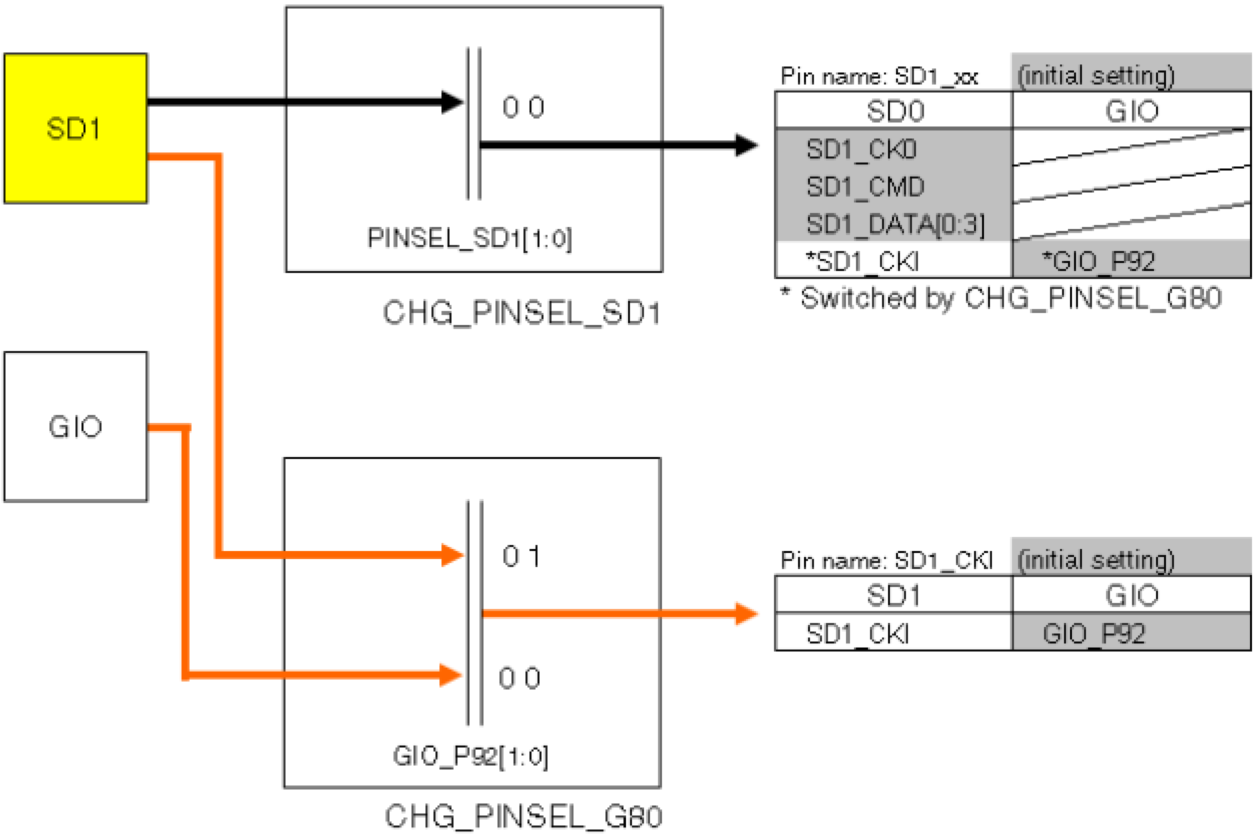
3.8.9. SD0



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G80 C014_0214	[31:30]	GIO_P95	PWM1			00b
	[29:28]	GIO_P94	PWM0			00b
	[27:26]	GIO_P93	SD2_CKI	NAND_OE		01b
	[25:24]	GIO_P92	SD1_CKI	CAM_CLKI		01b
	[23:22]	GIO_P91	SD0_CKI			01b
	[21:20]	GIO_P90	SD0_DATA3			01b
	[19:18]	GIO_P89	SD0_DATA2			01b
	[17:16]	GIO_P88	SD0_DATA1			01b
	[15:14]	GIO_P87	PM0_SI			01b
	[13:12]	GIO_P86	URT0_RTSB	URT1_SOUT		10b
	[11:10]	GIO_P85	URT0_CTSB	URT1_SRIN		10b
	[9:8]	GIO_P84	IIC_SDA			01b
	[7:6]	GIO_P83	IIC_SCL			01b
	[5:4]	GIO_P82	NTS_DATA7	PM1_SO	PM1_SO	01b
	[3:2]	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	01b
	[1:0]	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	01b

		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_SD0 C014_0288	[31:30]					
	[29:28]					
	[27:26]					
	[25:24]					
	[23:22]					
	[21:20]					
	[19:18]					
	[17:16]					
	[15:14]					
	[13:12]					
	[11:10]					
	[9:8]					
	[7:6]					
	[5:4]					
	[3:2]					
	[1:0]	SD0, GIO	SD0			00b

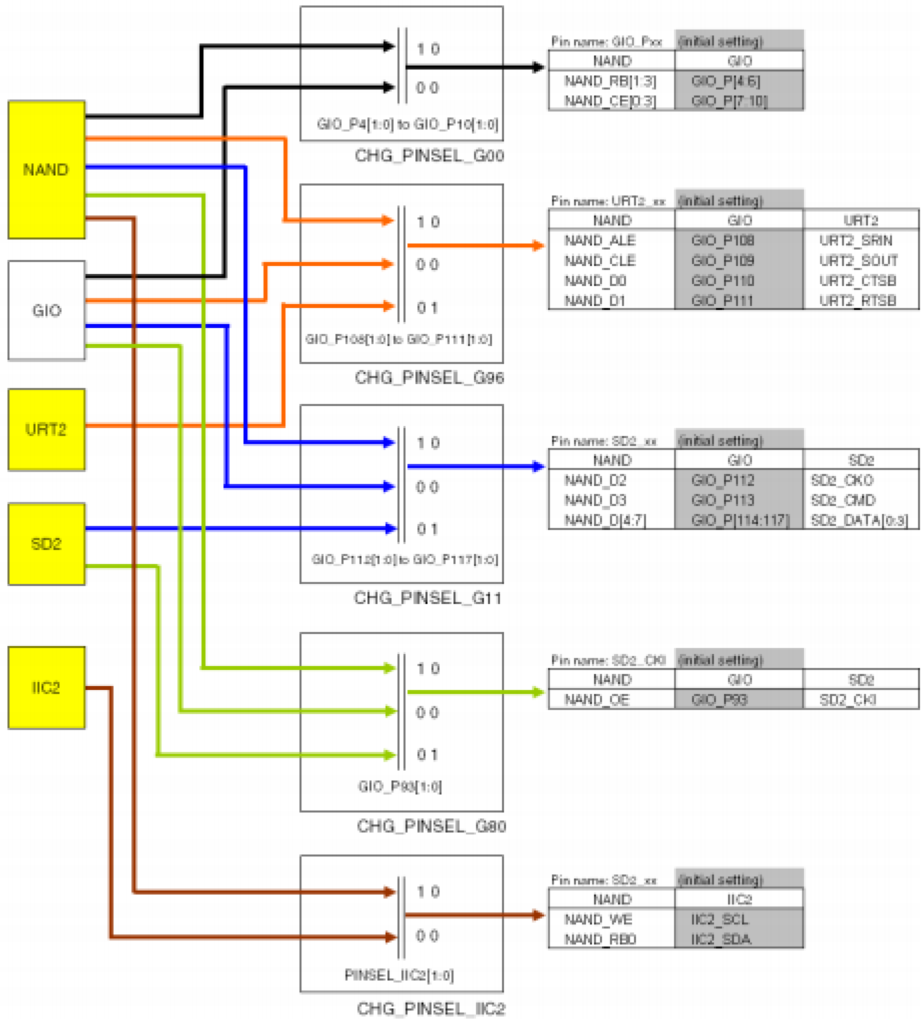
3.8.10. SD1



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G80 C014_0214	[31:30]	GIO_P95	PWM1			00b
	[29:28]	GIO_P94	PWM0			00b
	[27:26]	GIO_P93	SD2_CKI	NAND_OE		01b
	[25:24]	GIO_P92	SD1_CKI	CAM_CLKI		01b
	[23:22]	GIO_P91	SD0_CKI			01b
	[21:20]	GIO_P90	SD0_DATA3			01b
	[19:18]	GIO_P89	SD0_DATA2			01b
	[17:16]	GIO_P88	SD0_DATA1			01b
	[15:14]	GIO_P87	PM0_SI			01b
	[13:12]	GIO_P86	URT0_RTSB	URT1_SOUT		10b
	[11:10]	GIO_P85	URT0_CTSB	URT1_SRIN		10b
	[9:8]	GIO_P84	IIC_SDA			01b
	[7:6]	GIO_P83	IIC_SCL			01b
	[5:4]	GIO_P82	NTS_DATA7	PM1_SO	PM1_SO	01b
	[3:2]	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	01b
	[1:0]	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	01b

		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_SD1 C014_028C	[31:30]					
	[29:28]					
	[27:26]					
	[25:24]					
	[23:22]					
	[21:20]					
	[19:18]					
	[17:16]					
	[15:14]					
	[13:12]					
	[11:10]					
	[9:8]					
	[7:6]					
	[5:4]					
	[3:2]					
	[1:0]	SD1, GIO	SD1	CAM		00b

3.8.11. NAND, URT2, SD2, IIC



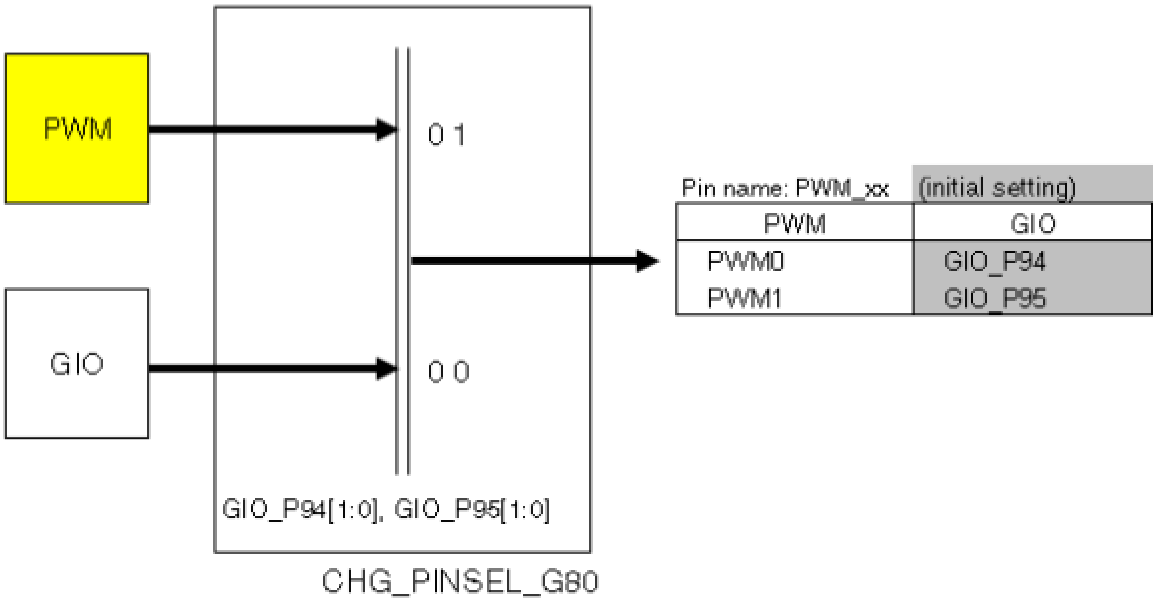
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G00 C014_0200H	[31:30]	GIO_P15	AB0_AD3			01b
	[29:28]	GIO_P14	AB0_AD2			01b
	[27:26]	GIO_P13	AB0_AD1			01b
	[25:24]	GIO_P12	AB0_AD0			01b
	[23:22]	GIO_P11	AB0_CLK	NTS_CLK		00b
	[21:20]	GIO_P10		NAND_CE3		00b
	[19:18]	GIO_P9		NAND_CE2		00b
	[17:16]	GIO_P8		NAND_CE1		00b
	[15:14]	GIO_P7		NAND_CE0		10b
	[13:12]	GIO_P6		NAND_RB3		00b
	[11:10]	GIO_P5		NAND_RB2		00b
	[9:8]	GIO_P4		NAND_RB1		00b
	[7:6]	GIO_P3				00b
	[5:4]	GIO_P2				00b
	[3:2]	GIO_P1	USB_WAKEUP	USB_PWR_FAULT		01b
	[1:0]	GIO_P0				00b

		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G96 C014_0218	[31:30]	GIO_P111	URT2_RTSB	NAND_D1		10b
	[29:28]	GIO_P110	URT2_CTSB	NAND_D0		10b
	[27:26]	GIO_P109	URT2_SOUT	NAND_CLE		10b
	[25:24]	GIO_P108	URT2_SRIN	NAND_ALE		10b
	[23:22]	GIO_P107	USB_NXT			01b
	[21:20]	GIO_P106	USB_STP			01b
	[19:18]	GIO_P105	USB_DIR			01b
	[17:16]	GIO_P104	USB_DATA7			01b
	[15:14]	GIO_P103	USB_DATA6			01b
	[13:12]	GIO_P102	USB_DATA5			01b
	[11:10]	GIO_P101	USB_DATA4			01b
	[9:8]	GIO_P100	USB_DATA3			01b
	[7:6]	GIO_P99	USB_DATA2			01b
	[5:4]	GIO_P98	USB_DATA1			01b
	[3:2]	GIO_P97	USB_DATA0			01b
	[1:0]	GIO_P96	USB_CLK			01b

		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G112 C014_021C	[31:30]					00b
	[29:28]					00b
	[27:26]					00b
	[25:24]					00b
	[23:22]					00b
	[21:20]					00b
	[19:18]					00b
	[17:16]					00b
	[15:14]	GIO_P119				00b
	[13:12]	GIO_P118				00b
	[11:10]	GIO_P117	SD2_DATA3	NAND_D7		01b
	[9:8]	GIO_P116	SD2_DATA2	NAND_D6		01b
	[7:6]	GIO_P115	SD2_DATA1	NAND_D5		01b
	[5:4]	GIO_P114	SD2_DATA0	NAND_D4		01b
	[3:2]	GIO_P113	SD2_CMD	NAND_D3		01b
	[1:0]	GIO_P112	SD2_CKO	NAND_D2		01b

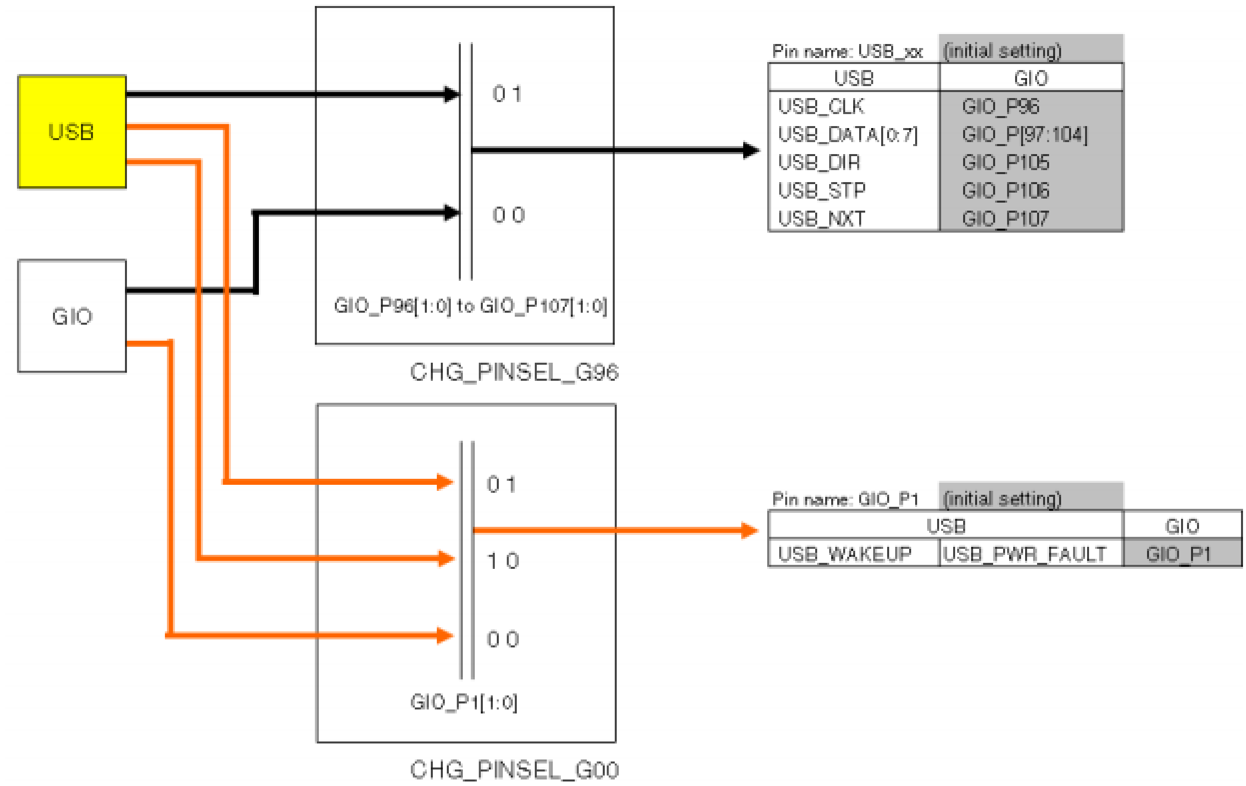
		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_IIC2 C014_0290	[31:30]					
	[29:28]					
	[27:26]					
	[25:24]					
	[23:22]					
	[21:20]					
	[19:18]					
	[17:16]					
	[15:14]					
	[13:12]					
	[11:10]					
	[9:8]					
	[7:6]					
	[5:4]					
	[3:2]					
	[1:0]	IIC2		NAND		10b

3.8.12. PWM



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G80 C014_0214	[31:30]	GIO_P95	PWM1			00b
	[29:28]	GIO_P94	PWM0			00b
	[27:26]	GIO_P93	SD2_CKI	NAND_OE		01b
	[25:24]	GIO_P92	SD1_CKI	CAM_CLKI		01b
	[23:22]	GIO_P91	SD0_CKI			01b
	[21:20]	GIO_P90	SD0_DATA3			01b
	[19:18]	GIO_P89	SD0_DATA2			01b
	[17:16]	GIO_P88	SD0_DATA1			01b
	[15:14]	GIO_P87	PM0_SI			01b
	[13:12]	GIO_P86	URT0_RTSB	URT1_SOUT		10b
	[11:10]	GIO_P85	URT0_CTSB	URT1_SRIN		10b
	[9:8]	GIO_P84	IIC_SDA			01b
	[7:6]	GIO_P83	IIC_SCL			01b
	[5:4]	GIO_P82	NTS_DATA7	PM1_SO	PM1_SO	01b
	[3:2]	GIO_P81	NTS_DATA6	SP1_CS5	PM1_SI	01b
	[1:0]	GIO_P80	NTS_DATA5	SP1_CS4	PM1_SEN	01b

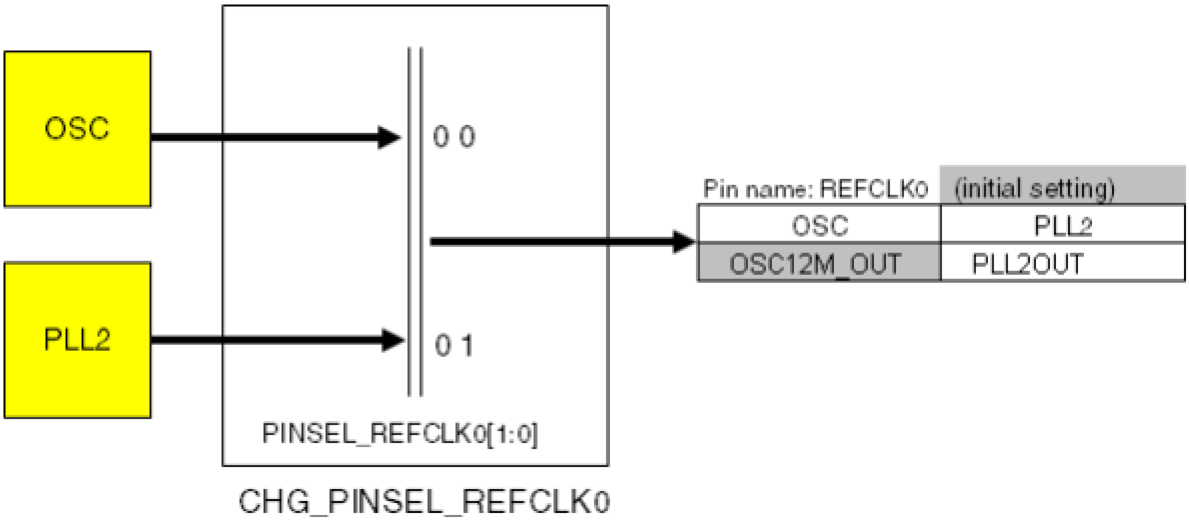
3.8.13. USB



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G96 C014_0218	[31:30]	GIO_P111	URT2_RTSB	NAND_D1		10b
	[29:28]	GIO_P110	URT2_CTSB	NAND_D0		10b
	[27:26]	GIO_P109	URT2_SOUT	NAND_CLE		10b
	[25:24]	GIO_P108	URT2_SRIN	NAND_ALE		10b
	[23:22]	GIO_P107	USB_NXT			01b
	[21:20]	GIO_P106	USB_STP			01b
	[19:18]	GIO_P105	USB_DIR			01b
	[17:16]	GIO_P104	USB_DATA7			01b
	[15:14]	GIO_P103	USB_DATA6			01b
	[13:12]	GIO_P102	USB_DATA5			01b
	[11:10]	GIO_P101	USB_DATA4			01b
	[9:8]	GIO_P100	USB_DATA3			01b
	[7:6]	GIO_P99	USB_DATA2			01b
	[5:4]	GIO_P98	USB_DATA1			01b
	[3:2]	GIO_P97	USB_DATA0			01b
	[1:0]	GIO_P96	USB_CLK			01b

		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_G00 C014_0200H	[31:30]	GIO_P15	AB0_AD3			01b
	[29:28]	GIO_P14	AB0_AD2			01b
	[27:26]	GIO_P13	AB0_AD1			01b
	[25:24]	GIO_P12	AB0_AD0			01b
	[23:22]	GIO_P11	AB0_CLK	NTS_CLK		00b
	[21:20]	GIO_P10		NAND_CE3		00b
	[19:18]	GIO_P9		NAND_CE2		00b
	[17:16]	GIO_P8		NAND_CE1		00b
	[15:14]	GIO_P7		NAND_CE0		10b
	[13:12]	GIO_P6		NAND_RB3		00b
	[11:10]	GIO_P5		NAND_RB2		00b
	[9:8]	GIO_P4		NAND_RB1		00b
	[7:6]	GIO_P3				00b
	[5:4]	GIO_P2				00b
	[3:2]	GIO_P1	USB_WAKEUP	USB_PWR_FAULT		01b
	[1:0]	GIO_P0				00b

3.8.14. OSC, PLL2



		alternative pins list				
Register	bit	00b	01b	10b	11b	set value
CHG_PINSEL_REFCLKO C014_0294	[31:30]					
	[29:28]					
	[27:26]					
	[25:24]					
	[23:22]					
	[21:20]					
	[19:18]					
	[17:16]					
	[15:14]					
	[13:12]					
	[11:10]					
	[9:8]					
	[7:6]					
	[5:4]					
	[3:2]					
	[1:0]	OSC12M_OUT	PLL2OUT			00b

3.9. Chip Select

3.9.1. EM1-S System Connection Architecture

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Table 3-7 EM1-S System Connection Architecture

EM1 I/F		IO Voltage	Board	Connected to:
PCM	PM0	VIO3	CPU	Codec LSI (AK4648)
	PM1	VIO3	IO	Expansion Connector CN4/5 (NTSC IF Pin Multiplexed)
SPI	SP0(CS0)	VIO3	CPU	DA9052 (For Control)
	SP0(CS1)	VIO3	IO	LCD (For LCD Panel Control)
	SP0(CS2)	-	-	Not Used
	SP1	VIO3	IO	Expansion Connector CN4/5 (NTSC IF Pin Multiplexed)
	SP2	VIO3	IO	Expansion Connector CN4/5 (DTV IF Pin Multiplexed)
DTV/DTV2		VIO3	IO	Expansion Connector CN4/5
BT656		VIO3	IO	NTSC Encoder → NTSC Out
AB0	CS0	VIO18	IO	NOR Flash
	CS1	VIO18	-	Not Used
	CS2	VIO18	IO	AB0 Connector
	CS3	VIO18	IO	Ether IF
SD	SD0	VIO3	CPU	microSD Card IF
	SD1	VIO3	IO	Expansion Connector CN4/5
	SD2	VIO3	CPU/IO	eMMC / NAND PAD
NAND		-	IO	NAND PAD
JTAG		VIO18/VIO3	CPU, IO	Mini-JTAG port on CPU Board, JTAG port (Mictor type) on IO Board
LCD		VIO18	CPU, IO	LCD Connector - Direct Connector on CPU Board, LCD Panel connection on IO Board
USB		VIO18	CPU	USB Phy → USB mini AB Connector
IIC	IIC	VIO3	CPU	Codec LSI (AK4648) on CPU Board, Expansion Connector CN4/5 on IO Board, GPIO Expander on IO Board
	IIC2	VIO3	IO	NAND PAD
UART	URT0	VIO3	CPU, IO	FT232(USB⇔Serial)Adaptation LSI on CPU Board, RS232_URT0 (IO Board) Expansion Connector CN4/5 on IO Board
	URT1	VIO3	-	Not Used
	URT2	VIO3	IO	NAND PAD
PWM		VIO3	-	Not Used
uWire		VIO3	-	Not Used
Camera		VIO18	IO	Expansion Connector CN4/5
GPIO	-	VIO18/VIO3	CPU, IO	(Please GPIO Spec Section)

Note: VIO3 and VIO18 are depended on DA9052 programming. The concrete voltage can refer to 3.3.2 EM1-DA9052 Connection

3.9.2. External Bus Chip Select (CSB0 to CSB3)

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Table 3-8 External Bus Chip Select (CSB0 to CSB3)

CS Number	Voltage[V] (Note 3)	Board	Connected to	Wait Register Address	Wait Value
CSB0	VIO18	IO	NOR Flash	AB0_CS0_WAITCTRL	0x02000502 (CSint=2, T2=0, T1=5, T0=2)
				AB0_CS0_WAITCTRLW	0x00010302 (T2_W=1, T1_W=3, T0_W=2)
CSB1	VIO18	IO	(Not used, CN3) Note1		
CSB2	VIO18	IO	(LAN9921 as GIO_P44) Note2		
CSB3	VIO18	IO	Ether IF (LAN9921)	AB0_CS3WAITCTRL	0x01000300 (CSint=1, T2=0, T1=3, T0=0)
				AB0_CS3WAITCTRL_W	0x00000300 (T2_W=0, T1_W=3, T0_W=0)

Note:
(1) CSB1 is not used in Design Kit Board but is connected to CN3 of IO board for external board.
(2) CSB2 of chip select signal is not used but it is connected to LAN9921-nRESET as GIO_P44 of alternating pin function
(3) VIO18 is depended on DA9052 programming. The concrete voltage can refer to 3.3.2 EM1-DA9052 Connection

3.9.3. SPI Chip Selects

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Table 3-9 SPI Chip Selects

SPx Number	Voltage [V] (Note)	Board	Connection
SP0（CS0）	VIO3	CPU	DA9052 （For Control）
SP0（CS1）	VIO3	IO	LCD（For LCD Panel Control）
SP0（CS2）	VIO3	-	（Not Used）
SP1	VIO3	IO	Expansion Connector CN5 （IO Board）
SP2	VIO3	IO	Expansion Connector CN4 （IO Board - Pin Multiplexed w/ DTVIF）

Note: VIO3 is depended on DA9052 programming. The concrete voltage can refer to 3.3.2 EM1-DA9052 Connection

3.10. IIC Connection

Table 3-10 IIC Read / Write Address

Device	Write Address (7bit*)	Read Address (7bit*)
AK4648	0x13 (0010011b)	0x13 (0010011b)
ADV7179	0x2B (0101011b)	0x2B (0101011b)
MAX7324	0x5D (1011101b)	0x6D (1101101b)

Note) Write and Read address do not include R/W bit of 8bit's LSB.

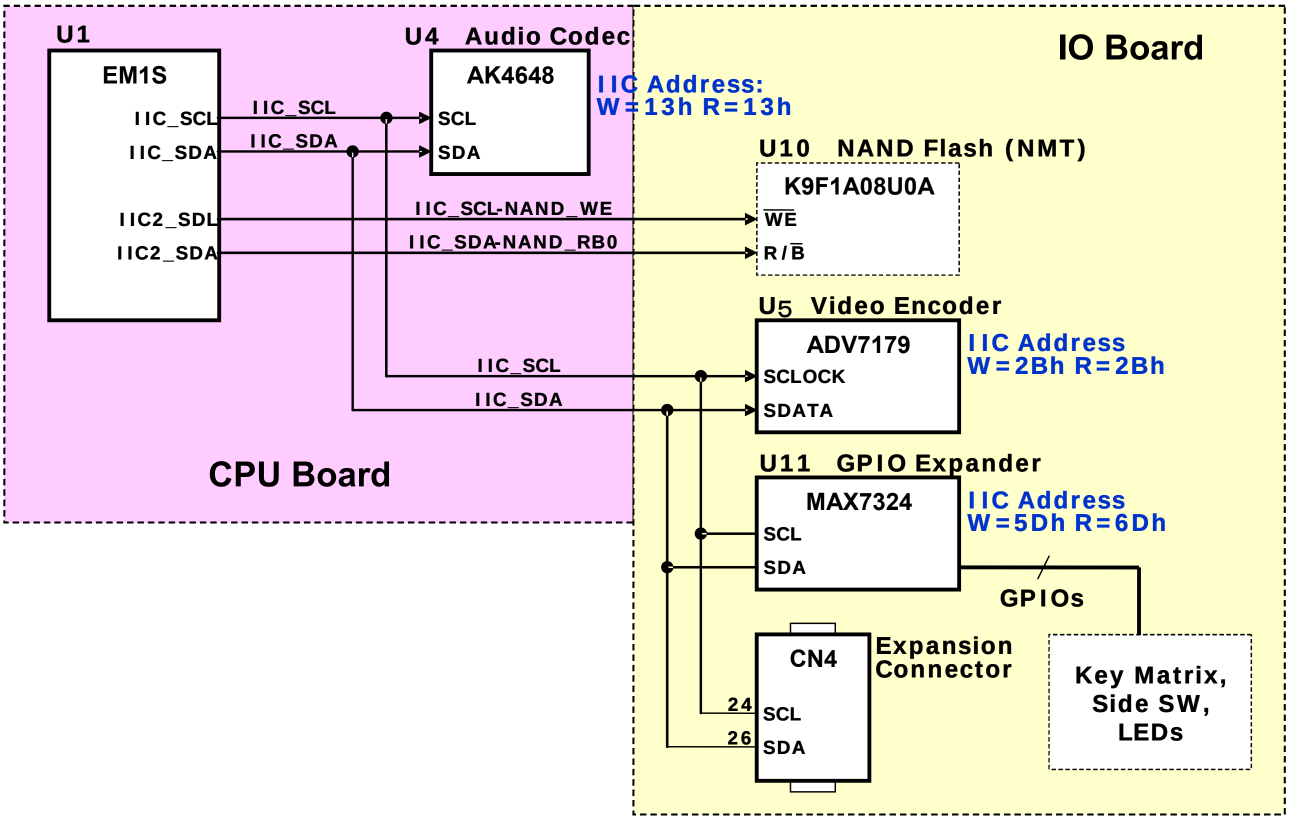


Figure 3-15 IIC Connection tree

3.11. Dip Switches, Keys, LED Specs

This section describes Power switches, Reset button, Push switches, General Purpose Matrix Key-buttons, Side Switches, and General Purpose LEDs. For DIP Switches, Please see Section x.x.

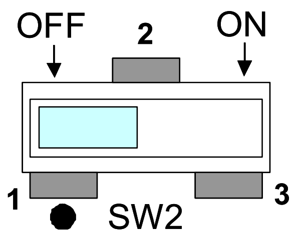
3.11.1. Button switches and LEDs on CPU Board

(1) Location

Please see 1.2.1: CPU Board Image.

(2) Specification

Table 3-11 CPU Board Button Switches

Switch & LED	Title	Type	GPIO Assign	Explanation
SW1	Board Reset Button	Push Type	―	Push Down: Reset Activated. For Details: Please See Reset System Section.
SW2	Debug Switch	Slide Type	―	Changes Debug Mode On: Debug Mode Off: Normal Mode  Fig. TOP View of SW2 (Debug On/OFF) You Should set SW2 to “ON” when you connect debugger ICE and use it.
SW3	―	―	―	（Not Used）
SW4	Multi Purpose Switch	Push Type	EM1 GIO_P36	Free Push Button for users Push Down: Activated. For Detail Architecture: Please see 3.9.3
SW5	Multi Purpose Switch	Push Type	EM1 GIO_P71	Free Push Button for uses Push Down: Activated. For Detail Architecture: Please see 3.9.3
LED1	Multi Purpose LED	Color: Green	DA9052 GPIO_14	Free LED for users For Detail Architecture: Please see 3.9.3
LED2	Multi Purpose LED	Color: Green	DA9052 GPIO_15	Free LED for users For Detail Architecture: Please see 3.9.3
LED3	Power LED	Color: Green	―	Power Indicator – VDDOUT line

3.11.2. Key-buttons, Side Switches, LEDs on IO Board

(1) Location – Key Matrix switch & General Purpose LEDs

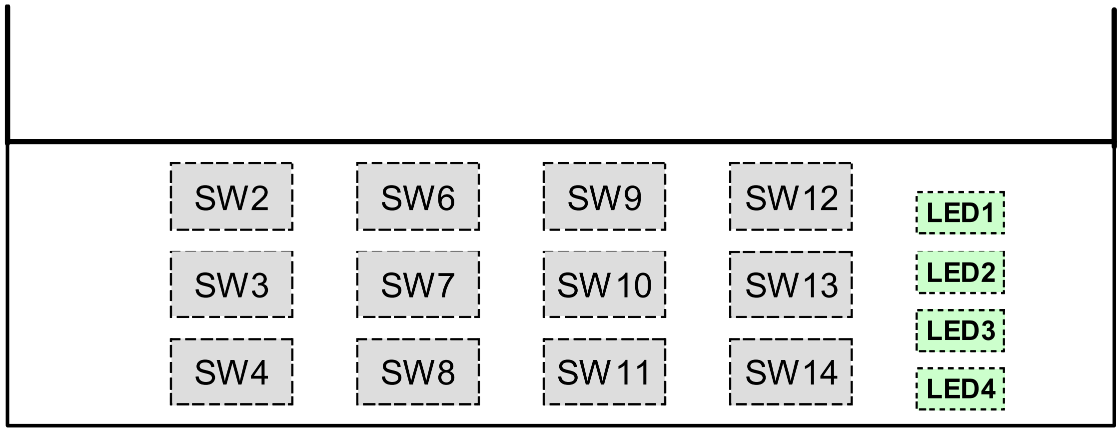


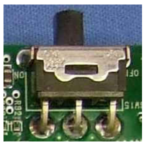
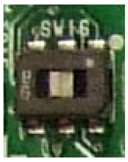
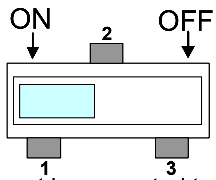
Figure 3-16 Top View of Key Matrix Switches and LEDs

(2) Location – Side Switches, other Switches

Please see 1.3.2 IO Board Image.

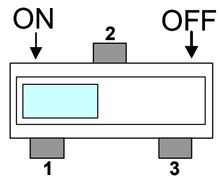
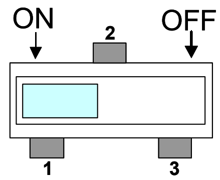
3.11.3. IO Board Switches and LEDs

Table 3-12 IO Board Switches and LEDs (1)

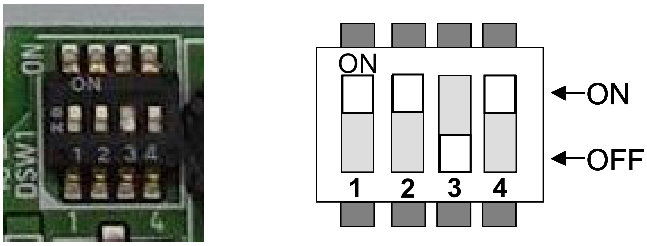
Switch & LEDs	Title	Type	GPIO Assign	Explanation
SW1,5	Side Switches	Push Type	(MAX7324)	Free Push Button Switches for users Push Down: Activated. Detail Architecture: Please see 3.9.3
SW2,3,4, 6,7,8, 9,,10,11, 12,13,14	Key Matrix Switches	Push Type	(MAX7324)	Free Push Button Switches for users Push Down: Activated. Detail Architecture: Please see 3.9.3
SW15	Power Switch	—	—	DC IN (AC Adapter) Power Switch ON OFF 
SW16	Debug Target Control Switch	Slide Type (DPDT)	—	Debug target switch: CPU or DSP ← DSP Debug  → CPU Debug This switch can change JTAG Signal assign to DSP or CPU.
SW17	NTS LSI Reset Switch	Slide Type (SPDT)	EM1 GIO_8	This switch can reset Video Encoder LSI ADV7179.  ON: ADV7179 Reset is connected to EM1 GIO_P8 OFF: ADV7179 Reset is connected to GND It can reduce useless current when NTSC/PAL function does not be used.
SW18	—	—	—	（Not Used）

(Continues to next Page)

Table 3-13 IO Board Switches and LEDs (2)

Switch & LEDs	Title	Type	GPIO Assign	Explanation
SW19	NTS/PM1 Clock Select	Slide Type (SPDT)	—	This Switch set NTSC 27MHz Clock supply to EM1 or not.  On: 27MHz Clock supply to EM1 OFF: 27MHz Clock not supply to EM1 This signal line is duplicated with PM1 Clock line (NTS_CLK-PM1_CLK). So SW19 should set to OFF when PM1 function is used. For Detail architecture, Please see 3.4.2.
SW20	USB Mode Select Switch	Slide Type (SPDT)	DA9052 GIO_1	This switch sets USB Mode.  On: USB IF is defined as DEVICE OFF: USB IF is defined as HOST
LED 1,2, 3,4	Multi Purpose LED	Color: Green	(MAX7324)	Free LED for users Detail Architecture: Please see 3.9.3
LED5	Power LED	Color: Green		Power Indicator – VDDOUT line

3.11.4. Boot Mode Switch (DSW1) on CPU Board



Example: SD Boot setting (ON/ON/OFF/ON)

Figure 3-17 DSW1 Photo and Top view Image

Table 3-14 DSW1 Boot Mode Switch Description (1)

No	DSW1-2	DSW1-3	DSW1-4	BOOT_SEL[2:0] Bit Setting	Description
1	ON	ON	ON	000b	NOR Boot
2	ON	ON	OFF	001b	eMMC Boot
3	ON	OFF	ON	010b	SD Boot
4	ON	OFF	OFF	011b	(Reserved)
5	OFF	ON	ON	100b	NAND Boot
6	OFF	ON	OFF	101b	AB0 boot (ADSP JTAG)
7	OFF	OFF	ON	110b	eMMC Boot (ADSP JTAG)
8	OFF	OFF	OFF	111b	SD Boot (ADSP JTAG)

Table 3-15 DSW1 Boot Mode Switch Description (2)

No	DSW1-1	BOOT_SEL3 Bit Setting	Description
1	OFF	1	L_SPEED mode ON
2	ON	0	L_SPEED mode OFF

For Detail Information for Change Boot mode register and its BOOT_SEL bit description: Please see EM1 1Chip Usert’s Manual.

3.11.5. General Purpose Key Buttons and LEDs System Architecture

(1) General Purpose Key Buttons System Architecture

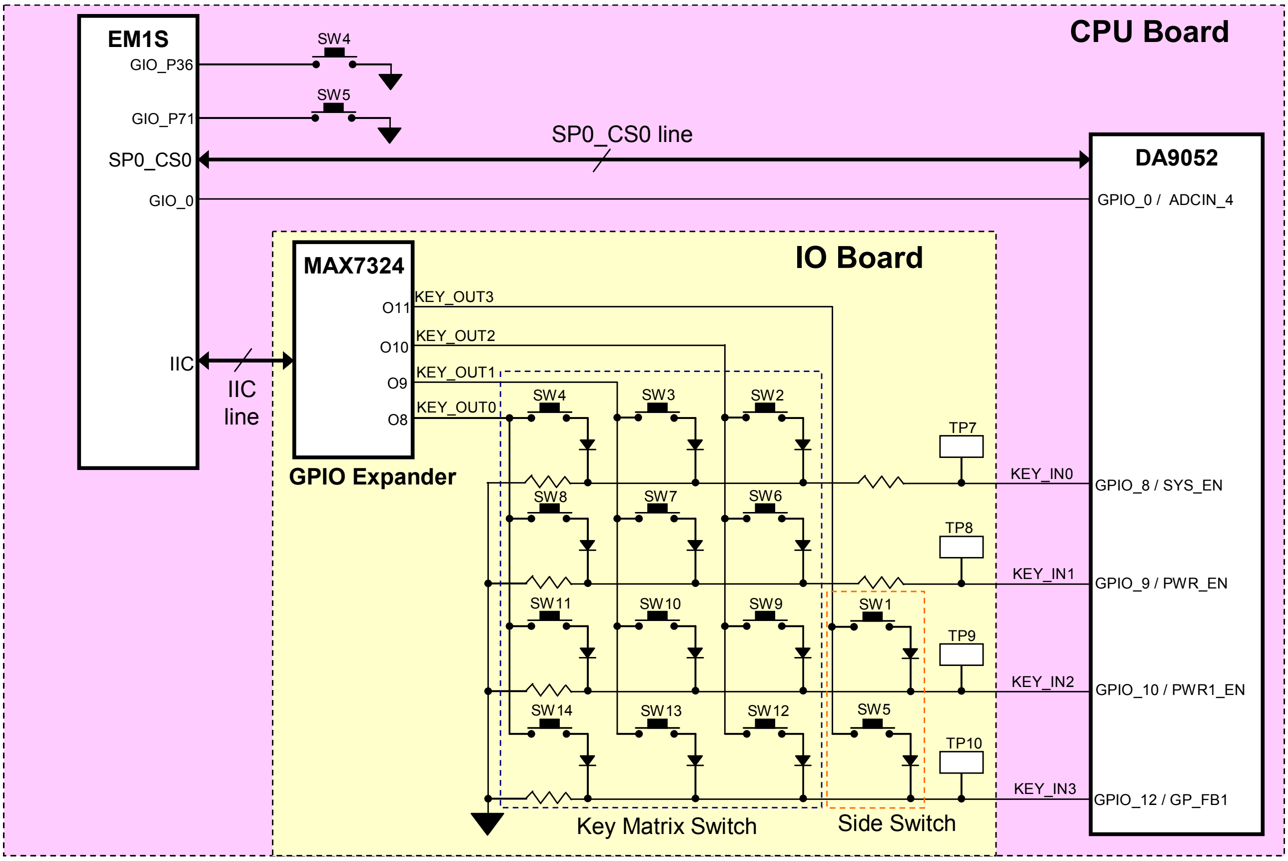


Figure 3-18 Key Buttons and Side Switch System

(2) General Purpose LEDs System Architecture

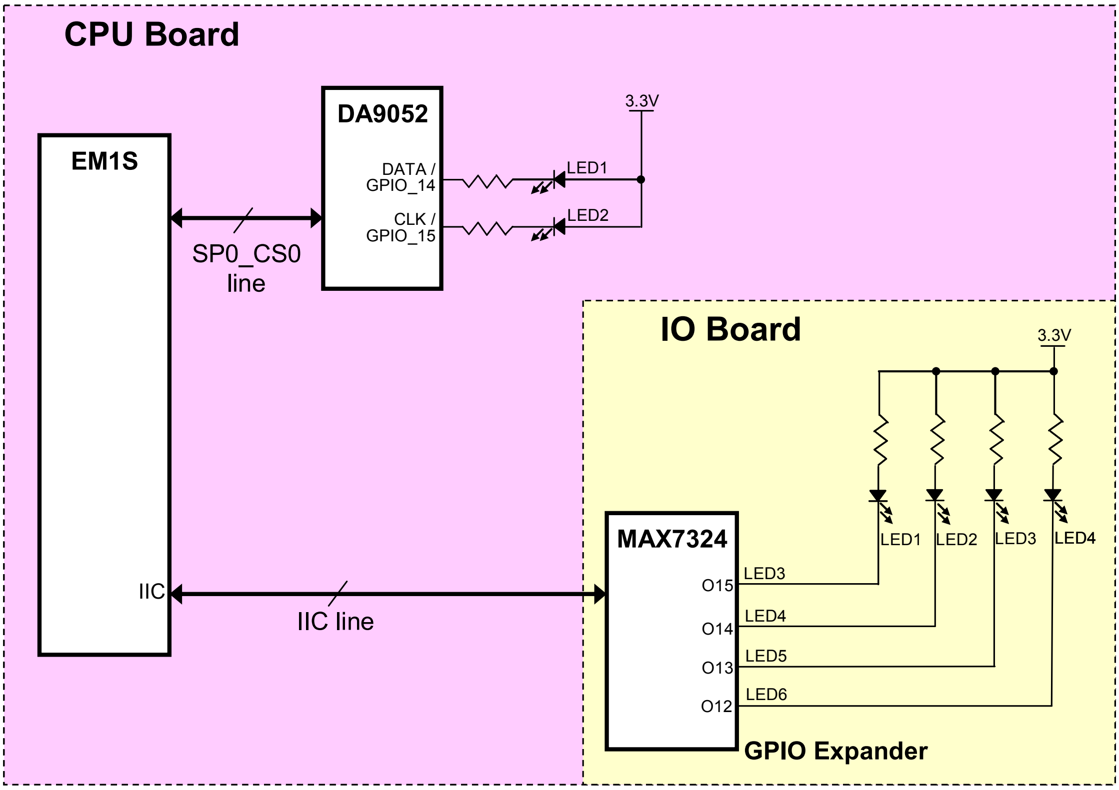


Figure 3-19 Key Buttons and Side Switch System

3.12. Audio LSI Connection

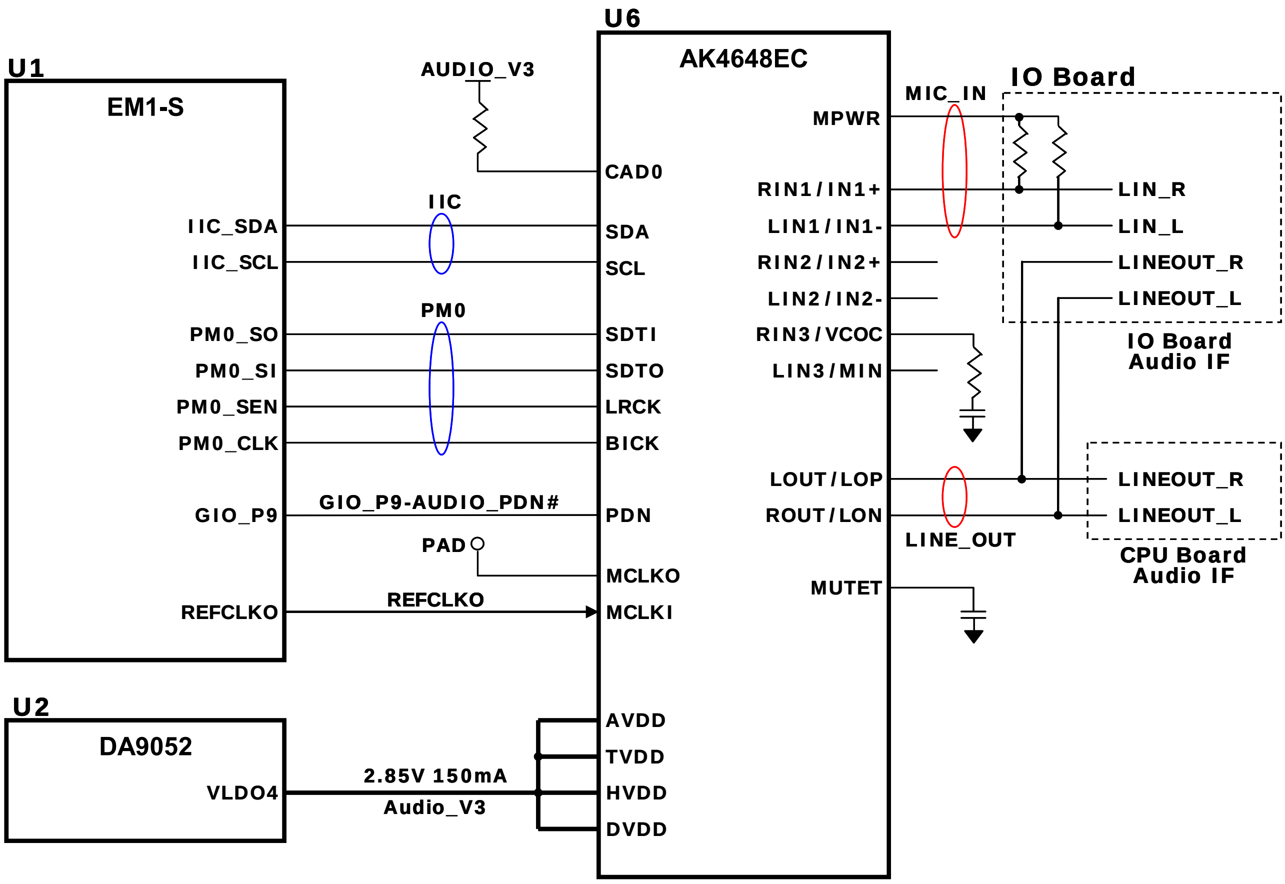


Figure 3-20 Audio IF Circuit Block Diagram

PDN: Power down mode: -H: Power Up, L: Power down. Reset and initialize the control register.

3.13. Lan9221 Connection with EM1

Lan9221 connection with EM1 is as follows: FIFO_SEL pin on LAN9221 is connected to AB0_11.

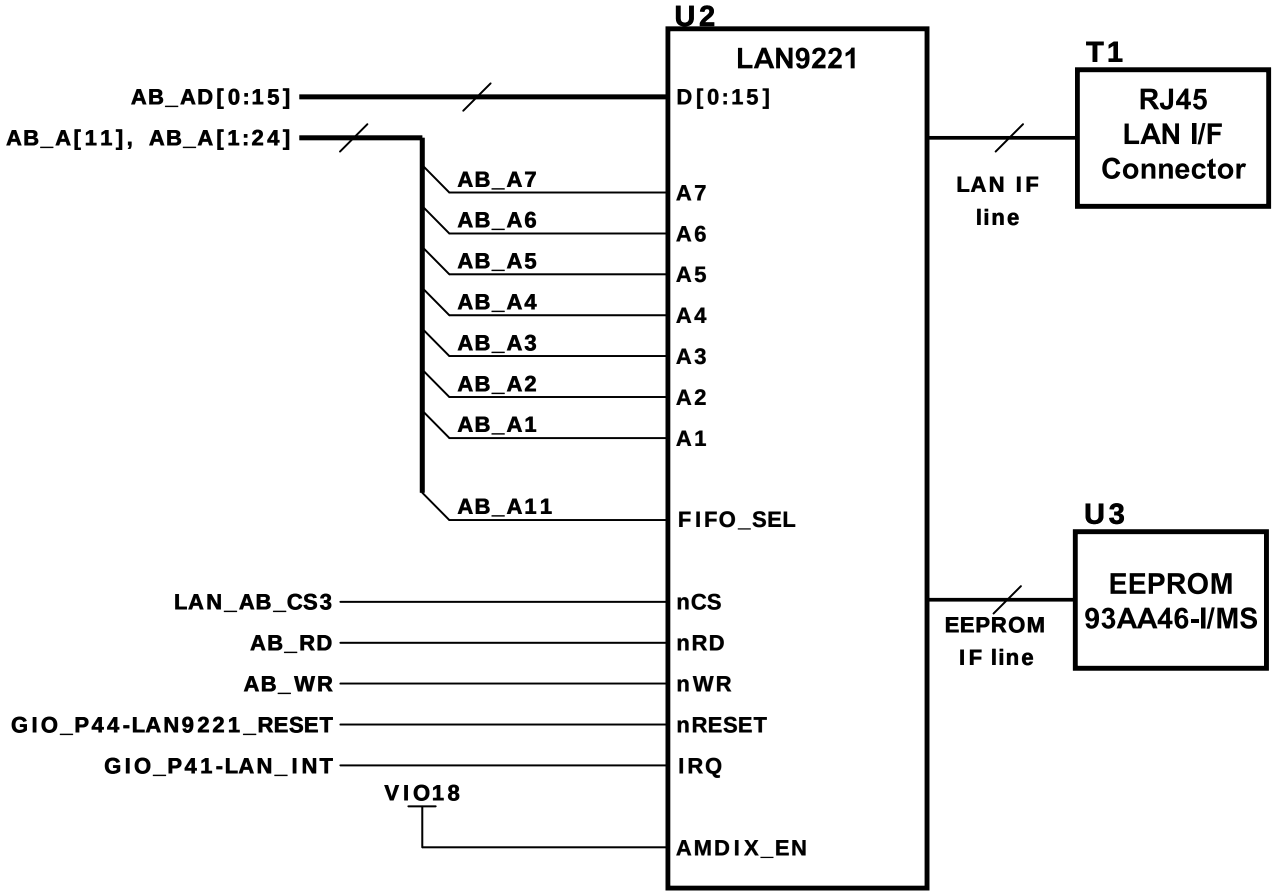


Figure 3-21 LAN9221- AB0 Connection

3.14. Touch Screen I/F

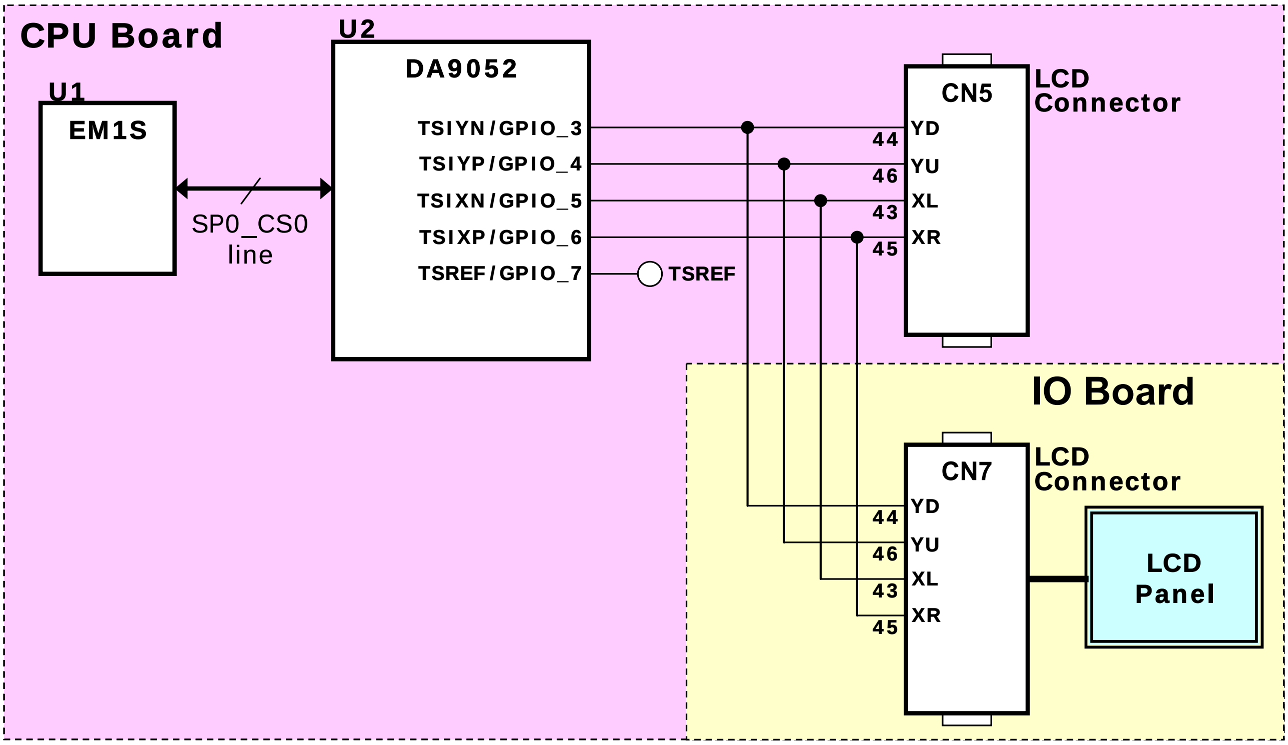
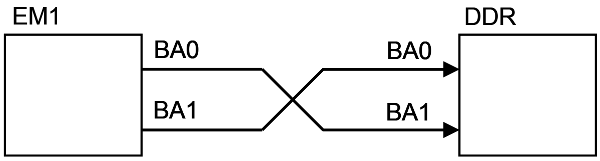


Figure 3-22 Touch Screen Control System

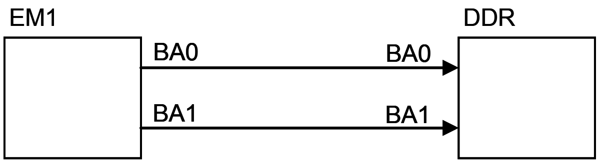
3.15. DDR Setting

BA0/BA1 signal connections are different by the board revision. The connections are two types as below. Please refer to 5.5 Board Revision about how to recognize. And these connections also can recognize by DDR-BA01 bit of EEPROM Address's 0x10 of LAN IC on software point of view. Please refer to 5.6 Board Information in EEPROM.

Board Rev 1
EEPROM 0x10 DDR-BA01 bit 5: 0



Board Rev 2
EEPROM 0x10 DDR-BA01 bit 5: 1



MEMC registers in next table is recommendation setting value. Regarding MEMC_DDR_CONFIGC1, it is different number related to Board revision. The EEPROM information can be confirmed by 5.6 Board Information in EEPROM.

	Address	Data
MEMC_DDR_CONFIGT2	0xC00A2024	0x14141414
MEMC_CLK270_SEL	0xC01101FC	0x00000000
MEMC_DDR_CONFIGT1	0xC00A2020	0x000F0A03
MEMC_DDR_CONFIGF	0xC00A2000	0x0000000F
MEMC_DDR_CONFIGA1	0xC00A2004	0x54443203
MEMC_DDR_CONFIGA2	0xC00A2008	0x20DA1042
MEMC_DDR_CONFIGC2	0xC00A2010	0x0000001D
MEMC_DDR_CONFIGC1	0xC00A200C	0x40200033 (EEPROM 0x10 DDR-BA01 bit 5: 0) 0x80200033 (EEPROM 0x10 DDR-BA01 bit 5: 1)
MEMC_DDR_CONFIGC2	0xC00A2010	0x00000018
MEMC_REQSCH	0xC00A1000	0x0000001F
MEMC_DDR_CONFIGC2	0xC00A2010	0x00000090
MEMC_DDR_CONFIGR1	0xC00A2014	0x00690069
MEMC_DDR_CONFIGR2	0xC00A2018	0x37771F1F(EEPROM 0x10 DDR bit3: 1) 0x37770101(EEPROM 0x10 DDR bit3: 0)
MEMC_DDR_CONFIGR3	0xC00A201C	0x00001415
MEMC_CACHE_MODE	0xC00A0000	0x00000100

Next table shows a recommendation number about related CHG register with MEMC.

	Address	Data
CHG_DRIVE0	0xC0140400	0xAAA002AA

3.16. SPI Interface

Development Kit board has SPI interface. The Chip select state can be confirmed at 3.9.3 SPI Chip Selects.
This section is described two notes as below.

- Maximum clock speed
Clock frequency of SPI interface is 14.28MHz maximum which is depend of a limit of DA9052 specification.

- PMIC DA9052 command order
DA9052 has two different of initial start-up by silicon revision. For common software, you need below.

Before SPI transmission between LCD panel and EM1, DA9052 shall supply LCD PS which is LDO5.
The register number is R54 and the value is 0x66. By the command, DA9052 LDO5 outputs 3.1V to LCD.

3.17. USB Interface

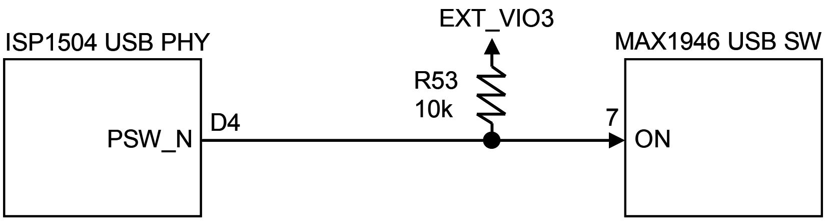
3.17.1. USB Switch for Host Mode

When you use USB Host mode, following switch and jumper switch must be set:

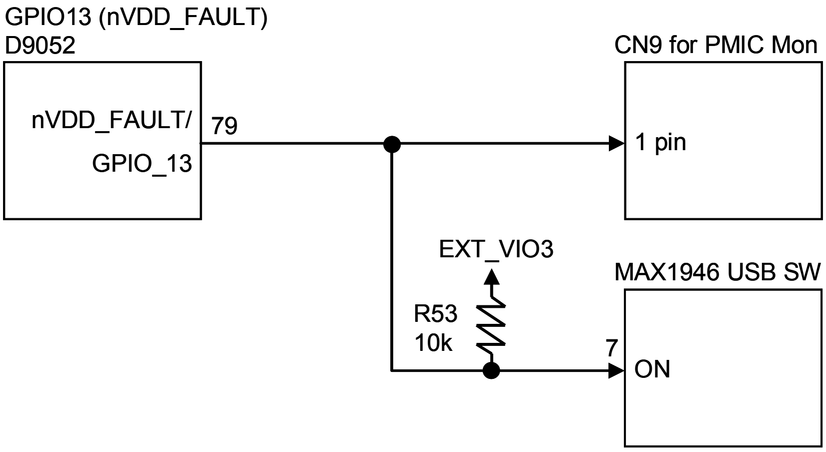
Board	Circuit Name	Setting	Note, refer to
CPU	JP1	USB Device: 2-3 short USB Host: 1-2 short	4.1.8 JUMPER[JP1]
IO	SW20	USB Device: ON (1-2 short) USB Host: : OFF (2-3 short)	Table 3-13 IO Board Switches and LEDs (2)

The Development Kit Board has a switch of VBUS voltage output for Host mode. The switch is controlled from two LSI depended on the board revision as below.

(1) Board revision: Rev1 (*)
The MAX1946 USB SW is controlled through ISP1504 USB PHY



(2) Board revision: Rev2 (*)
The MAX1946 USB SW is controlled through D9052 GPIO_13

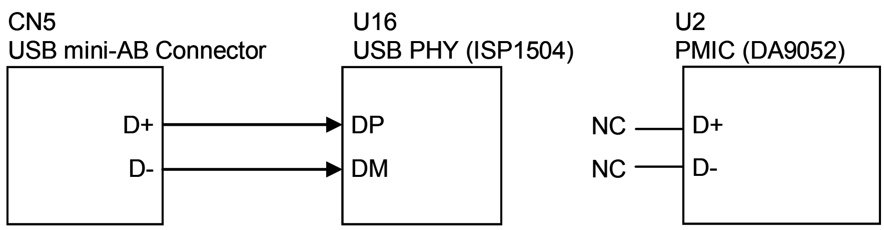


Note) Regarding Board revision, please refer to 5.5 Board Revision and 5.6 Board Information in EEPROM.

3.17.2. USB Charger Detection

Development Kit Board can detect USB Charger connection at DA9052 from board revision 2 as below. Regarding board revision, please refer to 5.5 Board Revision and 5.6 Board Information in EEPROM.

(1) Board revision 1



(2) Board revision 2

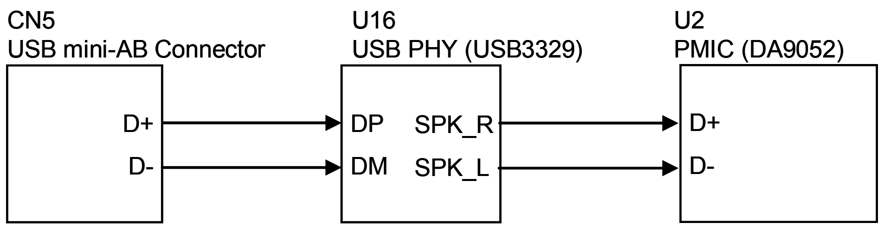


Table 3-16 DA9052 Register USB Charger Detection Setting

DA9052	Bit	Type	LABEL	OTP Rev. and Value	Board revision
R62	6	R/W	CHG_USB_ILIM	0 (r0.4/r0.4 modified)	Revision 1
R62	6	R/W	CHG_USB_ILIM	1 (r0.9)	Revision 2

CHG_USB_ILIM is automatic USB charger type detection. This function enables to detect by hardware before EM1 software working. When EM1 software starts after USB charger detection by hardware, EM1 software is suggested to set CHG_USB_ILIM=0 because the hardware detection of DA9052 is not needed on software working condition
.

CHAPTER 4. CONNECTORS

4.1. CPU Board Connectors

4.1.1. CCPU JTAG Connector [CN1]

Table 4-1 SICA20C20Y-GA102

PIN	Signal	PIN	Signal
1	VIO3	11	JT0_RTCK
2	VIO3	12	N.C.
3	JT0_TRSRZ	13	JTO_TDO
4	GND	14	GND
5	JT0_TDI	15	ICE_RESET
6	GND	16	GND
7	JT0_TMS	17	N.C.
8	GND	18	GND
9	JT0_TCK	19	N.C.
10	GND	20	GND

4.1.2. SD Interface Connector [CN2]

Table 4-2 DM3AT-SF-PEJ

PIN	Signal	PIN	Signal
1	DAT2	8	DAT1
2	CD/DAT3	9	A
3	CMD	10	B
4	VDD	11	N.C.
5	CLK	12	N.C.
6	VSS	13	N.C.
7	DAT0	14	N.C.

4.1.3. LCD Interface Connector [CN4]

Table 4-3 FH23-51S-0.3SHW(06)

PIN	Signal	PIN	Signal
1	GND	27	D20_R(GND)
2	VCC	28	D21_R(GND)
3	VCC	29	D22_R
4	VCC	30	D23_R
5	GND	31	D24_R
6	/RESET	32	D25_R
7	HSYNC	33	D26_R
8	VSYNC	34	D27_R
9	CLK	35	GND
10	GND	36	SCL
11	D00_B(GND)	37	SI
12	D01_B(GND)	38	SO
13	D02_B	39	/CS3
14	D03_B	40	VCOMIN
15	D04_B	41	VCCIO
16	D05_B	42	GND
17	D06_B	43	XL
18	D07_B	44	YD
19	D10_G(GND)	45	XR
20	D11_G(GND)	46	YU
21	D12_G	47	GND
22	D13_G	48	ANODE1
23	D14_G	49	CATHODE1
24	D15_G	50	ANODE2
25	D16_G	51	CATHODE2
26	D17_G		

4.1.4. USB Interface Connector [CN5]

Table 4-4 56579-0579

PIN	Signal	PIN	Signal
1	VBUS	6	SHIELD
2	D-	7	SHIELD
3	D+	8	SHIELD
4	ID	9	SHIELD
5	GND		

4.1.5. USB Interface (from UART) Connectors [CN6]

Table 4-5 UX60SA-MB-5ST

PIN	Signal	PIN	Signal
1	VBUS(N.C.)	6	SHIELD
2	D-	7	SHIELD
3	D+	8	SHIELD
4	ID(N.C.)	9	SHIELD
5	GND		

4.1.6. Peripheral Connector [CN7] [CN8]

Table 4-6 SO DIMM［CN7]

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	VBAT	41	GND	81	URT2_CTSB-NAND_D0	121	EXT_V12
2	VBAT	42	GND	82	URT2_RTSB-NAND_D1	122	EXT_V12
3	VBAT	43	GND	83	NAND_D2	123	EXT_V12
4	VBAT	44	GND	84	NAND_D3	124	EXT_V12
5	VBAT	45	AB_AD0	85	NAND_D4	125	EXT_V15
6	VBAT	46	AB_AD1	86	NAND_D5	126	EXT_V15
7	N.C.	47	AB_AD2	87	NAND_D6	127	EXT_V15
8	N.C.	48	AB_AD3	88	NAND_D7	128	EXT_V15
9	AB_A1	49	AB_AD4	89	GND	129	EXT_V18
10	AB_A2	50	AB_AD5	90	GND	130	EXT_V18
11	AB_A3	51	AB_AD6	91	NAND_OE	131	EXT_V18
12	AB_A4	52	AB_AD7	92	IIC2_SCL-NAND_WE	132	EXT_V18
13	AB_A5	53	GND	93	IIC2_SCL-NAND_RB0	133	EXT_V285
14	AB_A6	54	GND	94	GIO_P7-NAND_CE0#	134	EXT_V285
15	AB_A7	55	GND	95	URT2_SRIN-NAND_ALE	135	EXT_V285
16	AB_A8	56	GND	96	URT2_SOUT-NAND_CLE	136	EXT_V285
17	GND	57	AB_AD8	97	GIO_P6-NAND_WP#	137	VDDOUT
18	GND	58	AB_AD9	98	GND	138	VDDOUT
19	GND	59	AB_AD10	99	GND	139	VDDOUT
20	GND	60	AB_AD11	100	GND	140	VDDOUT
21	AB_A9	61	AB_AD12	101	KEY_IN0	141	LCD_3V
22	AB_A10	62	AB_AD13	102	KEY_IN1	142	LCD_3V
23	AB_A11	63	AB_AD14	103	KEY_IN2	143	LCD_3V
24	AB_A12	64	AB_AD15	104	KEY_IN3	144	LCD_3V
25	AB_A13	65	GND	105	GND	145	+5V
26	AB_A14	66	GND	106	GND	146	+5V
27	AB_A15	67	GND	107	GND	147	+5V
28	AB_A16	68	GND	108	GND	148	+5V
29	GND	69	NOR_AB_CS0	109	EXT_VIO3	149	+5V
30	GND	70	LAN_AB_CS3	110	EXT_VIO3	150	+5V
31	GND	71	EXT_AB_CS1	111	EXT_VIO3		
32	GND	72	AB_WR	112	EXT_VIO3		
33	AB_A17	73	AB_RD	113	VIO18		
34	AB_A18	74	AB_ADV	114	VIO18		
35	AB_A19	75	GND	115	VIO18		
36	AB_A20	76	GND	116	VIO18		
37	AB_A21	77	nRESET	117	NAND_V3		
38	AB_A22	78	nRESET_18	118	NAND_V3		
39	AB_A23	79	GND	119	NAND_V3		
40	AB_A24	80	GND	120	NAND_V3		

Table 4-7 SO DIMM［CN8］

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	GND	41	LCD_G5	81	EXT_URT0_SRIN	121	GIO_P4-CAM_STBY
2	GND	42	LCD_G4	82	URT0_SOUT	122	GIO_P49-CAM_RESETZ
3	GND	43	GND	83	URT1_SRIN	123	CAM_SCLK
4	GND	44	GND	84	URT1_SOUT	124	SD1_CKI_CAM_CLKI
5	YD	45	LCD_R1	85	GND	125	SD1_DATA3-CAM_HS
6	YU	46	LCD_R0	86	GND	126	SD1_DATA2-CAM_VS
7	XL	47	LCD_R3	87	GIO_P44-LAN9221_R	127	GND
8	XR	48	LCD_R2	88	GIO_P41-LAN_INT	128	GND
9	GND	49	LCD_R5	89	GND	129	SD1_DATA1-CAM_YUV7
10	GND	50	LCD_R4	90	GND	130	SD1_DATA0-CAM_YUV6
11	LED_CATHODE1	51	GND	91	NTS_DATA5-PM1_SE	131	SD1_CMD-CAM_YUV5
12	LED_CATHODE2	52	GND	92	NTS_DATA6-PM1_SI	132	SD1_DATA4-CAM_YUV4
13	GIO_P71-SW2	53	GND	93	NTS_DATA7-PM1_SO	133	NTS_DATA3-CAM_YUV3
14	LED_ANODE	54	GND	94	NTS_CLK-PM1_CLK	134	NTS_DATA2-SP1_CS1-
15	GND	55	GND	95	GND	135	NTS_DATA1-CAM_YUV1
16	GND	56	GND	96	GND	136	NTS_DATA0-SP1_SO-C
17	SP0_SI_18	57	N.C.	97	GND	137	AGND
18	SP0_CS1_18	58	N.C.	98	GIO_P10-WFI5	138	AGND
19	SP0_CLK_18	59	IIC_SDA	99	GIO_P10-WFI4	139	AGND
20	SP0_SO_18	60	IIC_SCL	100	GIO_P10-WFI3	140	MPWR
21	GND	61	GND	101	GIO_P10-WFI2	141	LIN1
22	GND	62	GND	102	GIO_P10-WFI1	142	RIN1
23	LCD_HSYNC	63	GND	103	GND	143	LINEOUT_L
24	LCD_VSYNC	64	ICE_RESET	104	GND	144	LINEOUT_R
25	GIO_P46-LCD_R	65	GND	105	GIO_P2-SD1_CD	145	AGND
26	LCD_PXCLK2	66	GND	106	SD1_CKO	146	AGND
27	GND	67	JT0_RTCK	107	NTS_VS-SP1_CLK	147	GND
28	GND	68	JT0_TRSTZ	108	NTS_HS-SP1_SI	148	TBAT
29	LCD_B1	69	JT0_TMS	109	GND	149	GND
30	LCD_B0	70	JT0_TDI	110	GND	150	GND
31	LCD_B3	71	JT0_TDO	111	EXT-OUT_32K		
32	LCD_B2	72	JT0_TCK	112	REFCLKO		
33	LCD_B5	73	GND	113	GND		
34	LCD_B4	74	GND	114	GND		
35	GND	75	USB_MODE-	115	DTV_DATA		
36	GND	76	D9052_GPIO	116	DTV_BCLK		
37	LCD_G1	77	GND	117	DTV_VLD		
38	LCD_G0	78	GND	118	DTV_PSYNC		
39	LCD_G3	79	GND	119	GND		
40	LCD_G2	80	GIO_P8-NTS	120	GND		

4.1.7. Power LSI (D9052) Monitor [CN9]

Pin 1 signal is different by the board revision. The connection is two types as below. Regarding Board Revision, please refer to 5.5 Board Revision.

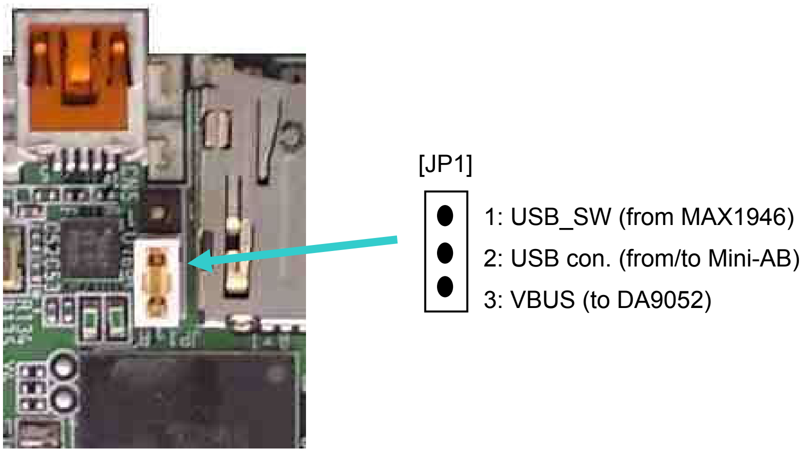
Table 4-8 BM07B-SRSS-TB

PIN	Signal	Board revision
1	nVDD Fault	Rev 1
	PSW_N	Rev 2
2	VBAT	
3	VDDCORE	
4	D9052_DATA	
5	D9052_CLK	
6	TP	
7	GND	

4.1.8. JUMPER [JP1]

Table 4-9 XJ3B-0311

SET	Setting
1-2	USB(HOST MODE)
2-3	USB(DEVICE MODE)



A photo of DEVICE Mode (2-3 set)

4.2. IO board Connectors

4.2.1. CPU Daughter Board Connectors [CN1, CN2]

Table 4-10 SO DIMM［CN1]

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	GND	41	LCD G5	81	EXT URT0 SRIN	121	GIO P4-CAM STBY
2	GND	42	LCD G4	82	URT0 SOUT	122	GIO P49-CAM RESETZ
3	GND	43	GND	83	URT1 SRIN	123	CAM SCLK
4	GND	44	GND	84	URT1 SOUT	124	SD1 CKI CAM CLKI
5	YD	45	LCD R1	85	GND	125	SD1 DATA3-CAM HS
6	YU	46	LCD R0	86	GND	126	SD1 DATA2-CAM VS
7	XL	47	LCD R3	87	GIO P44-LAN9221 R	127	GND
8	XR	48	LCD R2	88	GIO P41-LAN INT	128	GND
9	GND	49	LCD R5	89	GND	129	SD1 DATA1-CAM YUV7
10	GND	50	LCD R4	90	GND	130	SD1 DATA0-CAM YUV6
11	LED CATHODE1	51	GND	91	NTS DATA5-PM1 SE	131	SD1 CMD-CAM YUV5
12	LED CATHODE2	52	GND	92	NTS DATA6-PM1 SI	132	SD1 DATA4-CAM YUV4
13	GIO P71-SW2	53	GND	93	NTS DATA7-PM1 SO	133	NTS DATA3-CAM YUV3
14	LED ANODE	54	GND	94	NTS CLK-PM1 CLK	134	NTS DATA2-SP1 CS1-CA
15	GND	55	GND	95	GND	135	NTS DATA1-CAM YUV1
16	GND	56	GND	96	GND	136	NTS DATA0-SP1 SO-CA
17	SP0 SI 18	57	N.C.	97	GND	137	AGND
18	SP0 CS1 18	58	N.C.	98	GIO P10-WFI5	138	AGND
19	SP0 CLK 18	59	IIC SDA	99	GIO P10-WFI4	139	AGND
20	SP0 SO 18	60	IIC SCL	100	GIO P10-WFI3	140	MPWR
21	GND	61	GND	101	GIO P10-WFI2	141	LIN1
22	GND	62	GND	102	GIO P10-WFI1	142	RIN1
23	LCD HSYNC	63	GND	103	GND	143	LINEOUT L
24	LCD VSYNC	64	ICE RESET	104	GND	144	LINEOUT R
25	GIO P46-LCD R	65	GND	105	GIO P2-SD1 CD	145	AGND
26	LCD PXCLK2	66	GND	106	SD1 CKO	146	AGND
27	GND	67	JT0 RTCK	107	NTS VS-SP1 CLK	147	GND
28	GND	68	JT0 TRSTZ	108	NTS HS-SP1 SI	148	TBAT
29	LCD B1	69	JT0 TMS	109	GND	149	GND
30	LCD B0	70	JT0 TDI	110	GND	150	GND
31	LCD B3	71	JT0 TDO	111	EXT-OUT 32K		
32	LCD B2	72	JT0 TCK	112	REFCLKO		
33	LCD B5	73	GND	113	GND		
34	LCD B4	74	GND	114	GND		
35	GND	75	USB MODE-	115	DTV DATA		
36	GND	76	D9052 GPIO	116	DTV BCLK		
37	LCD G1	77	GND	117	DTV VLD		
38	LCD G0	78	GND	118	DTV PSYNC		
39	LCD G3	79	GND	119	GND		
40	LCD G2	80	GIO P8-NTS	120	GND		

Table 4-11 SO DIMM［CN2]

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	VBAT	41	GND	81	URT2_CTSB-NAND_D0	121	EXT_V12
2	VBAT	42	GND	82	URT2_RTSB-NAND_D1	122	EXT_V12
3	VBAT	43	GND	83	NAND_D2	123	EXT_V12
4	VBAT	44	GND	84	NAND_D3	124	EXT_V12
5	VBAT	45	AB_AD0	85	NAND_D4	125	EXT_V15
6	VBAT	46	AB_AD1	86	NAND_D5	126	EXT_V15
7	N.C.	47	AB_AD2	87	NAND_D6	127	EXT_V15
8	N.C.	48	AB_AD3	88	NAND_D7	128	EXT_V15
9	AB_A1	49	AB_AD4	89	GND	129	EXT_V18
10	AB_A2	50	AB_AD5	90	GND	130	EXT_V18
11	AB_A3	51	AB_AD6	91	NAND_OE	131	EXT_V18
12	AB_A4	52	AB_AD7	92	IIC2_SCL-NAND_WE	132	EXT_V18
13	AB_A5	53	GND	93	IIC2_SCL-NAND_RB0	133	EXT_V285
14	AB_A6	54	GND	94	GIO_P7-NAND_CE0#	134	EXT_V285
15	AB_A7	55	GND	95	URT2_SRIN-NAND_ALE	135	EXT_V285
16	AB_A8	56	GND	96	URT2_SOUT-NAND_CLE	136	EXT_V285
17	GND	57	AB_AD8	97	GIO_P6-NAND_WP#	137	VDDOUT
18	GND	58	AB_AD9	98	GND	138	VDDOUT
19	GND	59	AB_AD10	99	GND	139	VDDOUT
20	GND	60	AB_AD11	100	GND	140	VDDOUT
21	AB_A9	61	AB_AD12	101	KEY_IN0	141	LCD_3V
22	AB_A10	62	AB_AD13	102	KEY_IN1	142	LCD_3V
23	AB_A11	63	AB_AD14	103	KEY_IN2	143	LCD_3V
24	AB_A12	64	AB_AD15	104	KEY_IN3	144	LCD_3V
25	AB_A13	65	GND	105	GND	145	+5V
26	AB_A14	66	GND	106	GND	146	+5V
27	AB_A15	67	GND	107	GND	147	+5V
28	AB_A16	68	GND	108	GND	148	+5V
29	GND	69	NOR_AB_CS0	109	EXT_VIO3	149	+5V
30	GND	70	LAN_AB_CS3	110	EXT_VIO3	150	+5V
31	GND	71	EXT_AB_CS1	111	EXT_VIO3		
32	GND	72	AB_WR	112	EXT_VIO3		
33	AB_A17	73	AB_RD	113	VIO18		
34	AB_A18	74	AB_ADV	114	VIO18		
35	AB_A19	75	GND	115	VIO18		
36	AB_A20	76	GND	116	VIO18		
37	AB_A21	77	nRESET	117	NAND_V3		
38	AB_A22	78	nRESET_18	118	NAND_V3		
39	AB_A23	79	GND	119	NAND_V3		
40	AB_A24	80	GND	120	NAND_V3		

4.2.2. AB0 external [CN3]

Table 4-12 DF17(4.0)-60DS-0.5V(57)

PIN	Signal	PIN	Signal	PIN	Signal
1	EXT_V18	21	AB_A15	41	AB_AD6
2	EXT_V18	22	AB_A16	42	AB_AD7
3	EXT_V285	23	GND	43	GND
4	EXT_V285	24	GND	44	GND
5	AB_A1	25	AB_A17	45	AB_AD8
6	AB_A2	26	AB_A18	46	AB_AD9
7	AB_A3	27	AB_A19	47	AB_AD10
8	AB_A4	28	AB_A20	48	AB_AD11
9	AB_A5	29	AB_A21	49	AB_AD12
10	AB_A6	30	AB_A22	50	AB_AD13
11	AB_A7	31	AB_A23	51	AB_AD14
12	AB_A8	32	AB_A24	52	AB_AD15
13	GND	33	GND	53	NOR_AB_CS0
14	GND	34	GND	54	GND
15	AB_A9	35	AB_AD0	55	EXT_AB_CS1
16	AB_A10	36	AB_AD1	56	AB_RD
17	AB_A11	37	AB_AD2	57	AB_WR
18	AB_A12	38	AB_AD3	58	nRESET_18
19	AB_A13	39	AB_AD4	59	GND
20	AB_A14	40	AB_AD5	60	GND

4.2.3. Enhanced Connector [CN4]

Table 4-13 DF17(4.0)-40DS-0.5V(57)

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	GND	11	GND	21	DTV_VLD	31	EXT_V285
2	CAM_YUV1 (Note)	12	GND	22	GND	32	GND
3	GND	13	CAM_SCLK	23	DTV_PSYNC	33	EXT_V18
4	CAM_YUV3 (Note)	14	GND	24	IIC_SDA	34	EXT_V15
5	CAM_YUV4 (Note)	15	GND	25	GND	35	EXT_V18
6	GND	16	GND	26	IIC_SCL	36	VDDOUT
7	GND	17	DTV_DATA	27	DTV_BCLK	37	EXT_V12
8	GND	18	GIO_P49-CAM_RESETZ	28	GND	38	VDDOUT
9	GND	19	GND	29	GND	39	EXT_V12
10	GND	20	GIO_P4-CAM_STBY	30	REFCLKO	40	GND

<R>

Note) these signals are not connected to CN4 on default state IO board because the signal is alternate pin with NTS signal. For connection you need resistor mount to IO board. Regarding the modification, please refer to Modification for signals in external connector [CN4/CN5].

4.2.4. Enhanced Connector [CN5]

Table 4-14 DF17(4.0)-40DS-0.5V(57)

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	EXT-OUT_32K	11	SD1_DATA0-CAM_YUV6	21	UART2_SRIN	31	GND
2	GND	12	SP1_CS1-CAM_YUV2 (Note)	22	GIO_P11_WIFI2	32	NTS_CLK-PM1_CLK
3	SD1_CKI-CAM_CLKI	13	SD1_DATA1-CAM_YUV7	23	GND	33	UART2_RTSB
4	SP1_SI (Note)	14	GND	24	GIO_P94_WIFI3	34	GND
5	SD1_CKO	15	SD1_DATA2-CAM_VS	25	UART2_SOUT	35	GND
6	GND	16	SP1_CLK (Note)	26	GIO_P37_WIFI4	36	PM1_SI (Note)
7	SD1_CMD-CAM_YUV5	17	SD1_DATA3-CAM_HS	27	GND	37	PM1_SEN (Note)
8	SP1_SO-CAM_YUV0 (Note)	18	GND	28	GIO_P10_WIFI5	38	GND
9	GIO_P2-SD1_CD	19	GND	29	UART2_CTSB	39	GND
10	GND	20	GIO_P95_WIFI1	30	GND	40	PM1_SO (Note)

<R>

Note) these signals are not connected to CN5 on default state IO board because the signal is alternate pin with NTSC signal. For connection you need resistor mount to IO board. Regarding the modification, please refer to Modification for signals in external connector [CN4/CN5]

4.2.5. Debugger [CN6] [CN9]

Table 4-15 2-5767004-2

PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
1	(N.C.)	11	TDO	21	nTRST	31	GND
2	(N.C.)	12	Vref	22	GND	32	GND
3	(N.C.)	13	RTCK	23	GND	33	GND
4	(N.C.)	14	Vcc	24	GND	34	GND
5	GND	15	TCK	25	GND	35	GND
6	GND	16	GND	26	GND	36	GND
7	(N.C.)	17	TMS	27	GND	37	GND
8	GND	18	GND	28	GND	38	GND
9	ICE_RESET	19	TDI	29	GND	CG1	GND
10	pull up	20	GND	30	GND	CG2	GND
						CG3	GND
						CG4	GND
						CG5	GND

4.2.6. Battery Connector [CN10]

Table 4-16 Through Hole

PIN	Signal
1	VBAT
2	TBAT
3	GND



†For Using battery; Please contact "battery suppler or battery consultants" and DIALOG Semiconductor.

‡Europe Dialog Semiconductor GmbH Neue Strasse 95 D-73230 Kirchheim/Teck-Nabern Germany Phone: (+49) 7021 805-0 Fax: (+49) 7021 805-100 Email: dialog.nabern@diasemi.com Web: http://www.diasemi.com	‡North America Dialog North America 440 Oakmead Parkway Sunnyvale, CA 94085 USA Phone: (+1) 888-809-3816 Fax: (+1) 408-328-9275 Email: NA_sales_enquiries@diasemi.com
‡Japan Dialog Semiconductor K.K. Mita Kokusai Bldg 16F 1-4-28, Mita, Minato-ku, Tokyo, 108-0073 Japan Phone: (+81) 3 3769-8123 Fax: (+81) 3 3769-8124 Email: dialog.tokyo@diasemi.com	‡Taiwan Dialog Semiconductor GmbH Taiwan Branch Chu-Nan 3rd Factory No. 118 Chung-Hua Road Chu-Nan, Miao-Li 350 Taiwan R.O.C. Phone: +886 37 598 166 Fax: +886 37 595 026 Email: dialog.taiwan@diasemi.com

4.2.7. JTAG Connector [CN11]

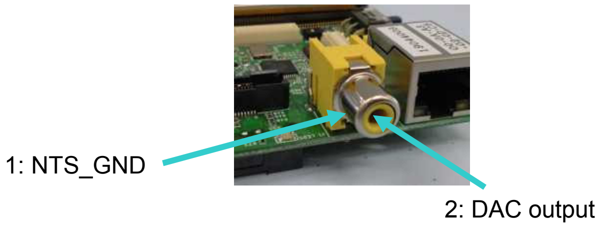
Table 4-17 FFC-12BMEP1

PIN	Signal
1	TRST
2	GND
3	JT0_TMS
4	GND
5	JT0_TDI
6	GND
7	TCK
8	GND
9	GND
10	N.C.
11	TDO
12	GND

4.2.8. NTSC/PAL Connector [J1]

Table 4-18 MR-551L

PIN	Signal
1	NTS_GND
2	DAC output



4.2.9. AUDIO Connector [J2, J3]

Table 4-19 M03-772A0 [J2]

PIN	Signal
1	RIN1
2	LIN1
3	AGND

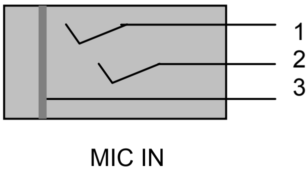
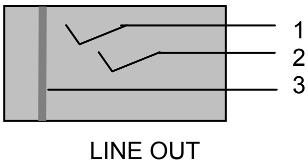


Table 4-20 M03-772A0 [J3]

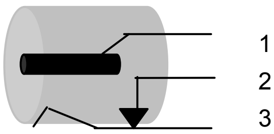
PIN	Signal
1	LINE_OUT_R
2	LINE_OUT_L
3	AGND



4.2.10. AC Adapter Connector [J4]

Table 4-21 HEC3600-010520

PIN	Signal
1	+5V
2	—
3	GND



Type: EIAJ 2
Input: 5V-2A

4.3. LCD

4.3.1. LCD Panel Interface Connector [CN7]

Table 4-22 FH23-51S-0.3SHW(06)

PIN	Signal	PIN	Signal	PIN	Signal
1	GND	21	D12_G	41	VCCIO
2	VCC	22	D13_G	42	GND
3	VCC	23	D14_G	43	XL
4	VCC	24	D15_G	44	YD
5	GND	25	D16_G	45	XR
6	/RESET	26	D17_G	46	YU
7	HSYNC	27	D20_R	47	GND
8	VSYNC	28	D21_R	48	ANODE1
9	CLK	29	D22_R	49	CATHODE1
10	GND	30	D23_R	50	ANODE2
11	D00_B	31	D24_R	51	CATHODE2
12	D01_B	32	D25_R	52	
13	D02_B	33	D26_R	53	
14	D03_B	34	D27_R	54	
15	D04_B	35	GND	55	
16	D05_B	36	SCL	56	
17	D06_B	37	SI	57	
18	D07_B	38	SO	58	
19	D10_G	39	/CS	59	
20	D11_G	40	VCOMIN	60	

CHAPTER 5. OTHERS

5.1. USB Connection

5.1.1. USB Mini B Connector by using serial COM port of EM1

USB Mini B connector is USB interface by using EM1 serial COM Port. EM1 URT0 is connected via FT232R (FTDI's USB-Serial Converter). PC connection is as follows;
5.1.1.1 Installation for “Virtual COM port driver” and “USB driver”
5.1.1.1.1 Download and extract above drivers from FTDI’s support site;
http://www.ftdichip.com/Drivers/D2XX.htm (At the time of May, 2009)
Click the version-number from “Driver Version” portion
5.1.1.1.2 Power-ON CPU and I/O boards
5.1.1.1.3 Connect USB mini B of CPU board to USB-A of PC by USB cable
5.1.1.1.4 If the PC detects “Unknown USB device”, you can set-up these drivers by PC’s instruction.
5.1.1.2 Connect PC and CPU and I/O boards via COM port
5.1.1.2.1 Power-ON CPU and I/O boards
5.1.1.2.2 Connect USB mini B of CPU board to USB-A of PC by USB cable
5.1.1.2.3 Start “Terminal Software” (ex. Hyper Terminal, Tera-Term)
5.1.1.3. An example of PC terminal software settings
Serial COM port:
Depend on “Virtual COM port driver” installation
Serial COM port Settings for Board Test Program:
Baud Rate: 115.2k, Data: 8bit, Parity: none, Stop bit: 1 bit
Flow Control: none (Fixed, CTS/RTS lines are short-circuited)
Note) above terminal-software settings are depend on board-software settings.

	“Virtual COM port driver” and “USB driver” are maintained / supported by FTDI (Future Technology Devices International Limited). If you have any trouble for above settings, please ask to FTDI directly.

Future Technology Devices International Limited (On May ’09)
Unit 1, 2 Seaward Place
Centurion Business Park
Glasgow
G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758
E-Mail (Support): support1@ftdichip.com
E-Mail (General Enquiries): admin1@ftdichip.com
Web Site URL: http://www.ftdichip.com

5.1.2. USB Mini AB

The Development Kit Board can receive a power supply voltage from USB Mini AB Connecter. This function needs a Jumper Switch set. But a supply current from USB Host is not enough for the Development Kit Board as CPU board, IO board and LCD panel.

5.2. Board installation to the Case

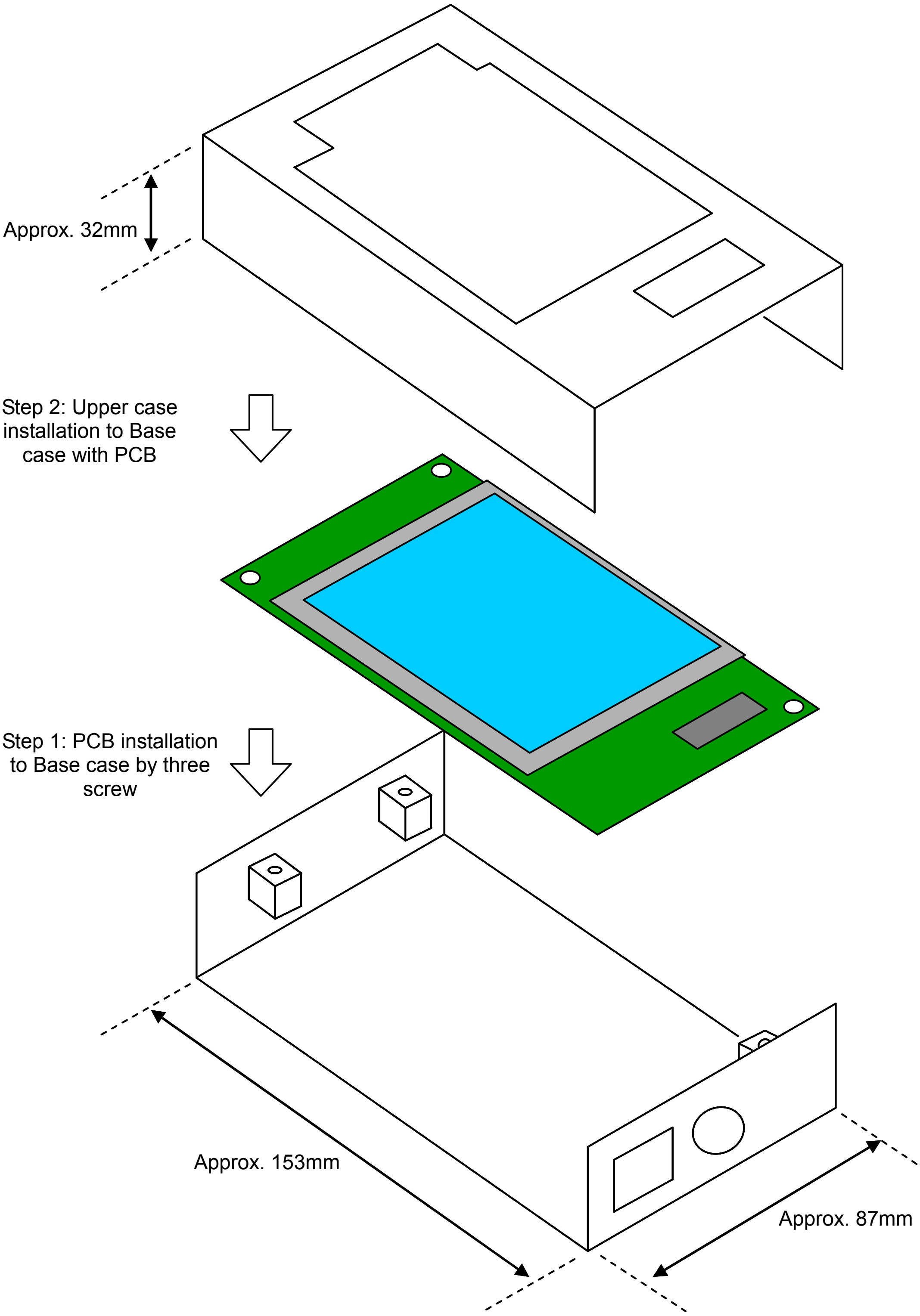


Figure 5-1 Case

5.3. MAC Address

MAC(MAC Address) sticker is on board.

Do not remove a MAC Address sticker.
Image：TBD

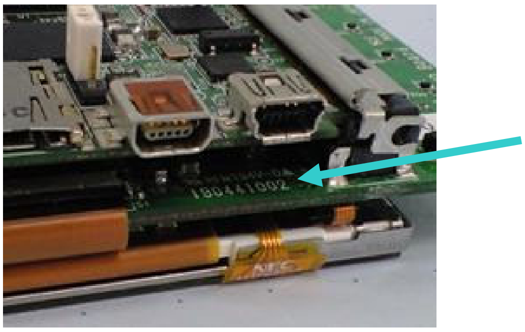
5.4. Serial Number

S/N (Serial Number) sticker is on board.

Do not remove a S/N (Serial Number) sticker.
Image：TBD

5.5. Board Revision

Board revision can be confirmed a character on PCB as below:



Information of Board revision
190441002: Rev 1
190441002A: Rev 2

There is a case that some mounting components are different by a revision of the board. Please refer to BOM of the board about the detail information. And recognition way for software of board revision can be confirmed in 5.6 Board Information in EEPROM.

5.6. Board Information in EEPROM (Factory setting)

Development Kit board has information for clarification of board revision on software point of view. And the information is related on Board Revision.
The information is in EEPROM of Ether IC (LAN9221) in IO board as below.

Do not overwrite any data in Board information. These data are needed for software to work normally.

<R>

Table 5-1 LAN9221 EEPROM Address: 0x10

7	6	5	4	3	2	1	0
EM1-S/D	USB-PHY	DDR-BA01	eMMC	Reserved			

Name	R*	Bits	Contents
EM1-S/D	R	7	EM1 device name on board 0: EM1-S 1: EM1-D
USB-PHY	R	6	USB-PHY device name on board 0: NXP ISP1504 1: SMSC USB3329
DDR-BA01	R	5	Two connection between EM1 and DDR 0: BA0-BA1 and BA1-BA0 1: BA0-BA0 and BA1-BA1
eMMC	R	4	eMMC device name on board 0: Micron MTFC4GDKDI 1: Samsung KMCEG0000A
DDR	R	3	DDR device name on board 0: Micron MT46H32M32LF without Auto Self Refresh function 1:TBD with Auto Self Refresh function
Reserved	R	2-0	Reserved.

Table 5-2 LAN9221 EEPROM Address: 0x11

7	6	5	4	3	2	1	0
PMIC rev			PMIC OTP			Reserved	

Name	R*	Bits	Contents
PMIC rev	R	7-5	PMIC device revision on board 000:DA9052 ES 001: DA9052 A silicon 010: DA9052 B silicon
PMIC OTP	R	4-2	OTP data of PMIC device for initial setting at factory. 000: DA9052 r0.4 001: DA9052 r0.4 modified 010: DA9052 r0.9
Reserved	R	2-0	Reserved.

Table 5-3 LAN9221 EEPROM Address: 0x12

7	6	5	4	3	2	1	0
NAND	BD1			BD2			

Name	R*	Bits	Contents
NAND	R	7	With/Without of NAND memory on IO board 0: Without NAND Flash memory 1: With NAND Flash memory
BD1	R	6-4	Board information Data 1 000: IO board revision 1 001: IO board revision 2 010-111: reserved
BD2	R	3-0	Board information Data 2, still not used 0000-1111: reserved

Note) Do not overwrite any data in Board information.

5.7. Monitor Point and Test Pad

Below table is shown points of monitor, test input or current measurement use which you can use, if it is necessary for you.
A current measurement point in table can be used for the current consumption measurement by using ampere meter. Signal monitor points in table can monitor by using oscilloscope or equivalent equipment.
Test input points are for use of functionality expansion.

<R>

Table 5-4 Monitor Point and Test Pad

Board Name	Purpose of Use	Name	Contents
CPU	Current measurement	R128 R139	These resistors are 0 ohm and are mounted on 1.2v line for EM1.
		R131	The resistor is 0 ohm and is mounted on 1.8v line for EM1 VIO18.
		R133	The resistor is 0 ohm and is mounted on 2.85v line for EM1 VIO3.
		R129	The resistor is 0 ohm and is mounted on 1.2V line for EM1 PLL circuit.
		R41 R42	These resistors are 0 ohm and are mounted on VBUS line from USB Mini-AB connector.
IO	Current measurement	R92 R96	These resistors are 0 ohm and are mounted on 5.0v line from AC adapter.
		R93 R97	These resistors are 0 ohm and are mounted on VBAT line to/from CN10 which is NMT and for a battery connection.
CPU	Signal Monitor	TP1	AK4648 MCKO
		TP2	D9052 VPERI_SW
		TP3	D9052 VMEM_SW
		TP4	D9052 PWR_UP
		TP5	D9052 GPIO_0
IO	Signal Monitor	TP4	URT0_SRIN_R (ADM3202)
		TP5	URT0_SOUT_R (ADM3202)
	GND	TP6	GND Pad
	Signal Monitor	TP7	KEY_IN0 (DA9052 GPIO_8)
		TP8	KEY_IN1 (DA9052 GPIO_9)
		TP9	KEY_IN2 (DA9052 GPIO_10)
		TP10	KEY_IN3 (DA9052 GPIO_12)
		TP11	URT1_SOUT (EM1)
		TP12	URT1_SRIN (EM1)
		TP14	D9052_GPIO_0
		TP15	CPU Board SW5 (EM1 GIO_P71)
	Input for Test	TP16	IIC Expander input 0 (MAX7324)
		TP17	IIC Expander input 1 (MAX7324)
		TP18	IIC Expander input 2 (MAX7324)
		TP19	IIC Expander input 3 (MAX7324)
		TP20	IIC Expander input 4 (MAX7324)
		TP21	IIC Expander input 5 (MAX7324)
		TP22	IIC Expander input 6 (MAX7324)
		TP23	IIC Expander input 7 (MAX7324)
	GND	TP24	GND Terminal

<R>

5.8. Modification for signals in external connector [CN4/CN5]

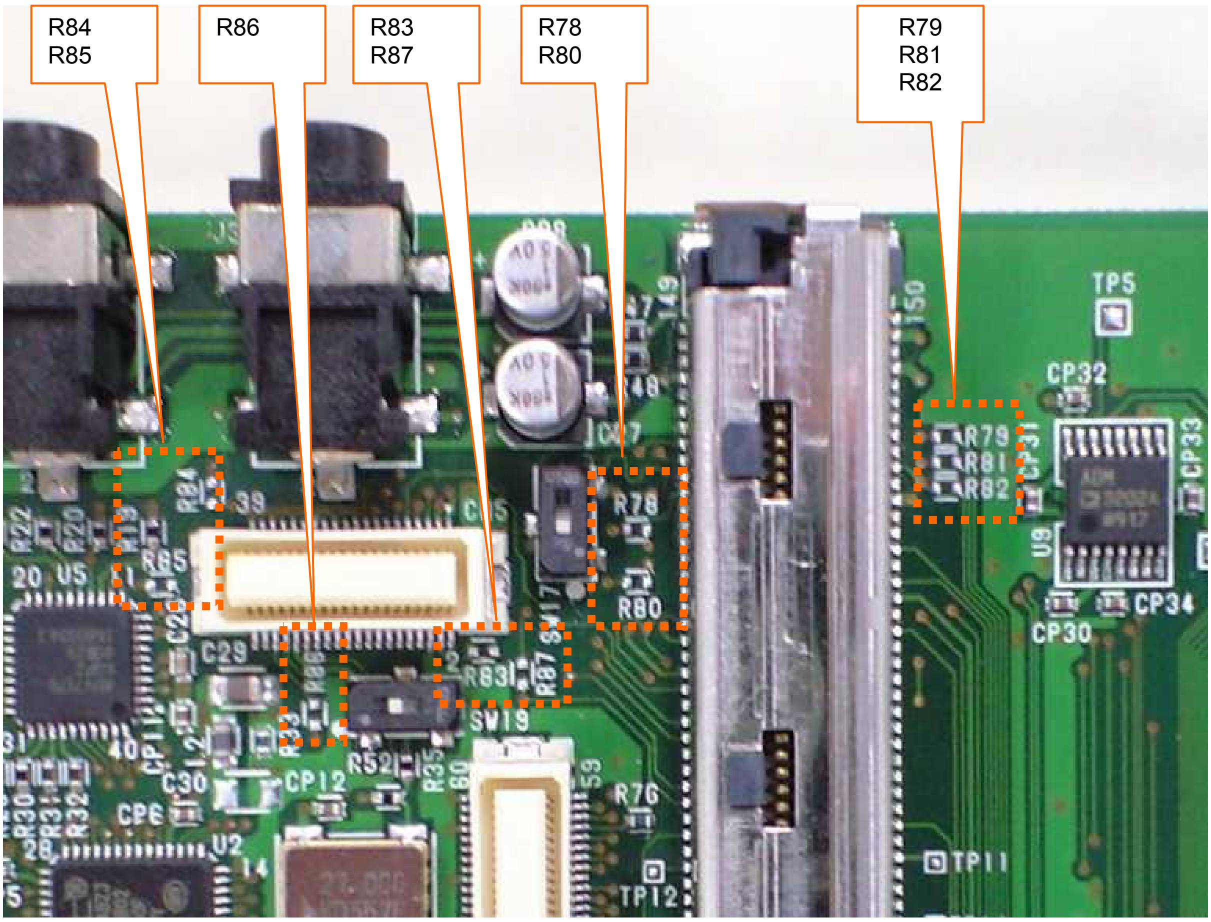
Following table shows modification point for connection to external connector. Alternate signals of NTSC signal is not connected on default state's IO board. So when any signal of the table is used through external connector [CN4/CN5], it needs modification to use it. And after the modification, please refer to Connection of CPU board and IO board for connection of CPU and IO board.

Table 5-5 Modification signal in external connector

Board	Connector	Signal	Resistor	Default (Note 1)	Modification for use case	Alternate signal (Note 2)
IO	CN4	CAM_YUV1	R78	NMT	0 ohm	NTS_DATA1
		CAM_YUV3	R79	NMT	0 ohm	NTS_DATA3
		CAM_YUV4	R80	NMT	0 ohm	NTS_DATA4
	CN5	SP1_SO-CAM_YUV0	R81	NMT	0 ohm	NTS_DATA0
		SP1_CS1-CAM_YUV2	R82	NMT	0 ohm	NTS_DATA2
		SP1_SI	R83	NMT	0 ohm	NTS_HS
		SP1_CLK	R84	NMT	0 ohm	NTS_VS
		PM1_SO	R85	NMT	0 ohm	NTS_DATA7
		PM1_SI	R86	NMT	0 ohm	NTS_DATA6
		PM1_SEN	R87	NMT	0 ohm	NTS_DATA5

Note1. NMT means "not mounted component".
Note2. After the modification, please take care about output signal's wired-or. Alternate signal cannot use at the same time. For the example, CAM_YUV1 from camera component and NTS_DATA1 from EM1 is output signal. You should not use camera interface and NTSC interface after the modification.

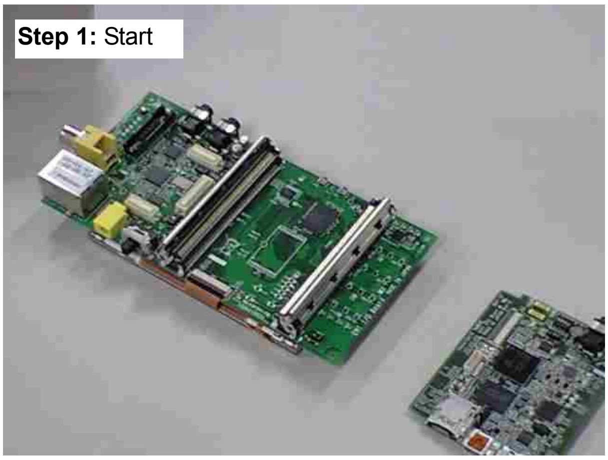
Regarding place of R78-R87, please refer to following photo.



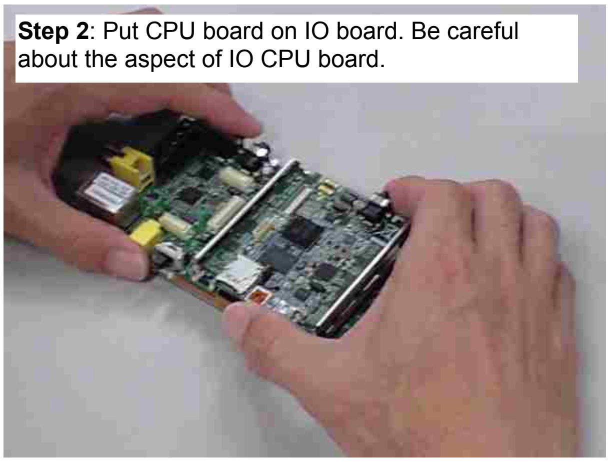
<R>

5.9. Connection of CPU board and IO board

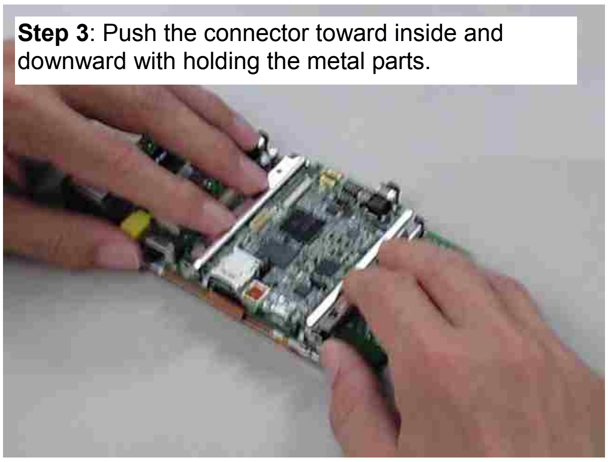
CPU board and IO board is connected by two couple of 150 pin connectors. If you detach the connectors for a reason, please carefully refer to a following procedure for attaching the connectors.



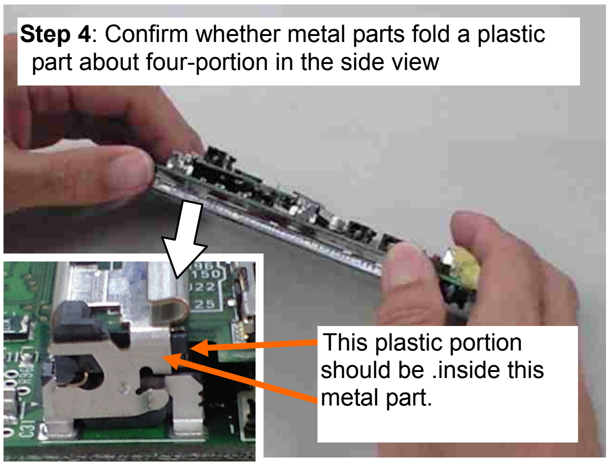
Step 1: Start



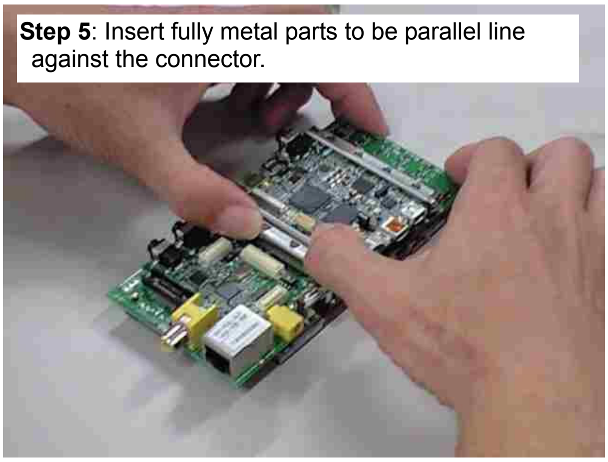
Step 2: Put CPU board on IO board. Be careful about the aspect of IO CPU board.



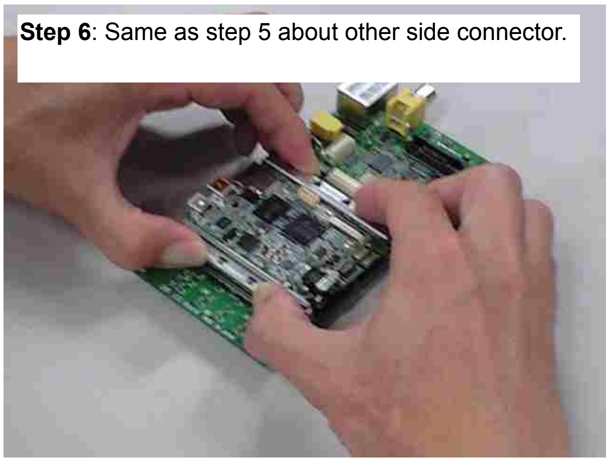
Step 3: Push the connector toward inside and downward with holding the metal parts.



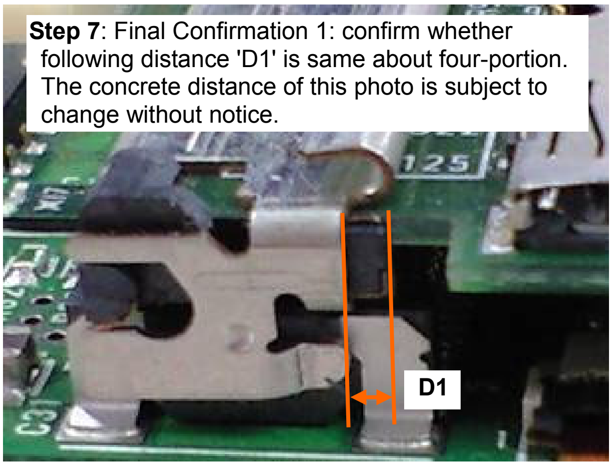
Step 4: Confirm whether metal parts fold a plastic part about four-portion in the side view



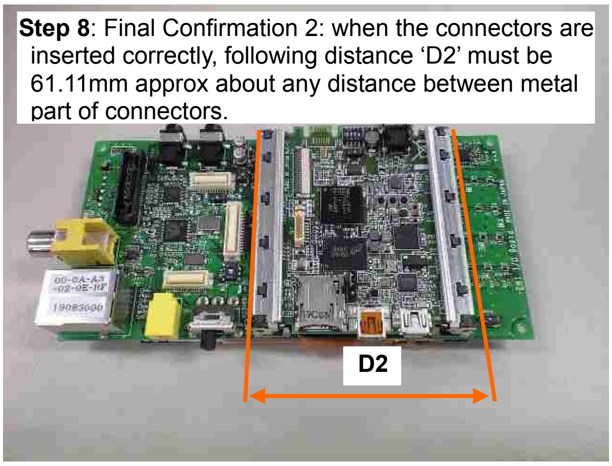
Step 5: Insert fully metal parts to be parallel line against the connector.



Step 6: Same as step 5 about other side connector.



Step 7: Final Confirmation 1: confirm whether following distance 'D1' is same about four-portion. The concrete distance of this photo is subject to change without notice.



Step 8: Final Confirmation 2: when the connectors are inserted correctly, following distance ‘D2’ must be 61.11mm approx about any distance between metal part of connectors.

Revision history

Date	Revision	Comments	Writer
28th Oct. 2009	1.0	First edition	
4th Feb 2010	1.1	NEC Revision 2.3　を反映 NEC Revision 2.4　を反映	Arase
16th Feb 2010	1.2	表に以下を追加しました。 010: DA9052 B silicon	Urano
17th, Mar. 2010	1.3	**5.8 Modification for signals in external connector [CN4/CN5]** を新規追加 **5.9 Connection of CPU board and IO board** を新規追加 **4.2.3Enhanced Connector [CN4]** テーブル内に Note を追加 **4.2.4Enhanced Connector [CN4]** テーブル内に Note を追加 **5.2.Board installation to the Case** ケース寸法と外形図、取り付け方法を見直し **5.6 Board Information in EEPROM (Factory setting)** TTable 番号を取得(内容に変更なし) **5.7 Monitor Point and Test Pad** Table 番号を取得(内容に変更なし) **Revision History, Rev2.4** Revision History 2.4 版の位置を前の頁に移動	Arase
02nd, Apr. 2010		各頁　社名変更(NEC→Renesas) Table 5-2 LAN9221 EEPROM Address: 0x11 PMIC rev ビットに B silicon を追加 Table 5-3 LAN9221 EEPROM Address: 0x12 NAND ビット誤記訂正 (旧：0: With NAND memory 1: Without NAND memory)	